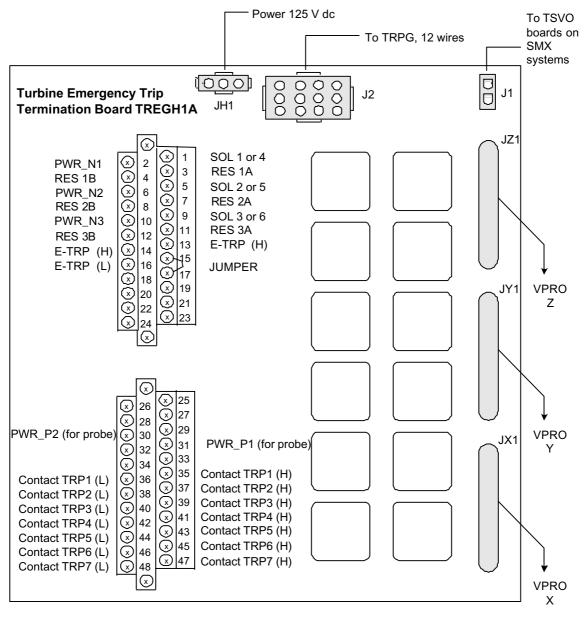
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Functional Description

VPRO also connects to the TPRO terminal board and has an Ethernet connection for IONet communications with the control modules. The VPRO board in the Protection Module <P> provides the emergency trip function. Up to three trip solenoids can be connected between the TREG and TRPG terminal boards. TREG provides the positive side of the 125 V dc to the solenoids and TRPG provides the negative side. VPRO provides emergency overspeed protection and the emergency stop functions. It controls the 12 relays on TREG, nine of which form three groups of three to vote inputs controlling the three trip solenoids. A second TREG board may be driven from VPRO through J4.

Installation

The three trip solenoids, economizing resistors, and the emergency stop are wired directly to the first I/O terminal block. Up to seven trip interlocks can be wired to the second terminal block. The wiring connections are shown in the following figure.



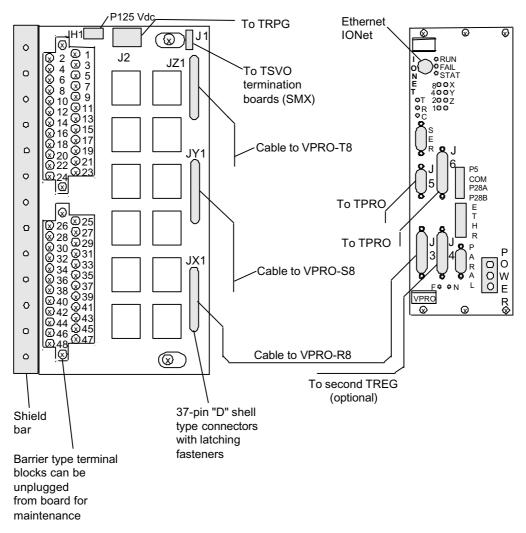
Up to two #12 AWG wires per point with 300 volt insulation

Terminal blocks can be unplugged from terminal board for maintenance

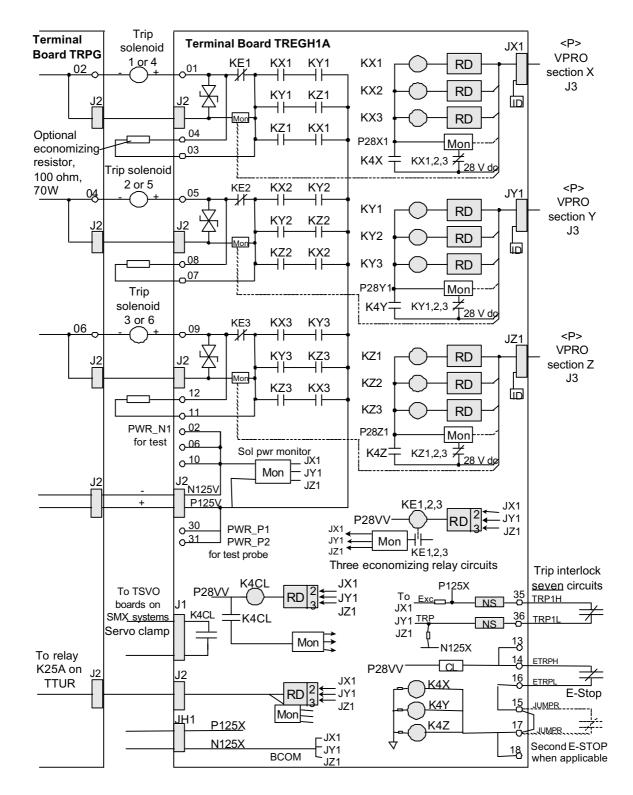
TREG Terminal Board

TREG Terminal Board

VPRO Module – R8



Trip Emergency Terminal Board, VPRO Board, and Cabling



TREG Board, Trip Interlocks, and Trip Solenoids

Operation

The solenoid circuit has a metal oxide varistor (MOV) for current suppression and a 10 ohm, 70 watt economizing resistor.

. A normally closed contact from each relay is used to sense the relay status for diagnostics TREG is entirely controlled by VPRO, and the only connections to the control modules are the J2 power cable and the trip solenoids. In Simplex systems a third cable carries a trip signal from J1 to the TSVO terminal board, providing a servo valve clamp function upon turbine trip.

Control of Trip Solenoids

Both TRPG and TREG control the trip solenoids so that either one can remove power and actuate the hydraulics to close the steam or fuel valves. The nine trip relay coils on TREG are supplied with 28 V dc from VPRO boards in X, Y, and Z. The trip solenoids are supplied with 125 V dc via plug J2, and draw up to 1 amp with a 0.1 second L/R time constant.

A separately fused 125 V dc feeder is provided from the turbine control for the solenoids which energize in the run mode and de-energize in the trip mode. Diagnostics monitor each 125 V dc feeder from the power distribution module at its point of entry on the terminal board to verify the fuse integrity and the cable connection.

Two series contacts from each emergency trip relay (ETR1, 2, 3) are connected to the positive 125 V dc feeder for each solenoid, and two series contacts from each primary trip relay (PTR1,2,3 in TRPG) are connected to the negative 125 V dc feeder for each solenoid. An economizing relay (KE1, 2, 3) is supplied for each solenoid with a normally closed contact in parallel with the current limiting resistor. These relays are used to reduce the current load after the solenoids are energized. The ETR and KE relay coils are powered from a 28 V dc source from the VPRO boards. Each VPRO board in each of the X, Y, and Z sections supplies an independent 28 V dc source.

The 28 V dc bus is current limited and used for power to an external manual emergency trip contact, shown as E-STOP. Three master trip relays (K4X, K4Y, K4Z) disconnect the 28 V dc bus from the ETR, and KE relay coils if a manual emergency trip occurs. Any trip which originates in either the protection module (such as EOS) or the TREG (such as a manual trip) will cause each of the three protection module sections to transmit a trip command over the IONet to the control module, and may be used to identify the source of the trip.

In addition, the K4CL servo clamp relay will energize and send a contact feedback directly from the TREG terminal board to the TSVO servo terminal board. TSVO disconnects the servo current source from the terminal block and applies a bias to drive the control valve closed. This is only used on Simplex applications to protect against the servo amplifier failing high. Note that the primary and emergency overspeed systems will trip the hydraulic trip solenoids independent of this circuit.

Solenoid Trip Tests

Application software in the control module is used to initiate tests of the trip solenoids. Online tests allow each of the trip solenoids to be manually tripped one at a time either through the PTR relays from the control module(s) or through the ETR relays from the protection module. A contact from each solenoid circuit is wired back as a contact input to give a positive indication that the solenoid has tripped. Primary and emergency offline overspeed tests are provided too for verification of actual trips due to software simulated trip overspeed conditions.

Specifications

Item	Specification
Number of trip solenoids (TREG)	Three solenoids per TREG (total of 6 per VPRO)
Trip solenoid rating	125 V dc standard with 1 A draw 24 V dc is alternate with 1 A draw
Trip solenoid circuits	Circuits rated for NEMA class E creepage and clearance Circuits can clear a 15 A fuse with all circuits fully loaded
Solenoid response time	Solenoid L/R time constant is 0.1 second
Suppression	MOV across the solenoid
Relay outputs	Three economizer relay outputs, two second delay to energize
	Driver to breaker relay K25A on TTUR
	Servo clamp relay on TSVO
Solenoid control relay contacts	Contacts are rated to interrupt inductive solenoid loads at 125 V dc, 1 A Bus voltage can vary from 70 to 145 V dc
Trip inputs	Seven trip interlocks to VPRO protection module, 125/24 V dc One emergency stop hardwired trip interlock, 24 V dc
Trip interlock excitation	H1 - Nominal 125 V dc, floating, ranging from 100 to 145 V dc H2 – Nominal 24 V dc, floating, ranging from 18.5 to 32 V dc
Trip interlock current	H1 for 125 V dc applications: Circuits draw 2.5 mA (50 kohms) H2 for 24 V dc applications: Circuits draw 2.5 mA (10 kohms)
Trip interlock isolation	Optical isolation to 1500 volts on all inputs
Trip interlock filter	Hardware filter, 4 ms
Trip interlock Ac voltage rejection	60 V rms @ 50/60 Hz at 125 V dc excitation

TREG Board Specifications

Diagnostics

Descriptions of the TREG diagnostics are contained in the VPRO section. The diagnostics cover the trip relay driver and contact feedbacks, solenoid voltage, economizer relay driver and contact feedbacks, K25A relay driver and coil, servo clamp relay driver and contact feedback, and the solenoid voltage source.

Connectors JX1, JY1, and JZ1 on the terminal board have their own ID device that is interrogated by the I/O board. The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and the plug location.

Configuration

TREG is configured using the toolbox. This software usually runs on a data-highway connected CIMPLICITY station or workstation. The following table summarizes the configuration choices and defaults. For details refer to GEH-6403 *Control System Toolbox for Configuring the Mark VI Turbine Controller*.

Parameter	Description	Choices
Configuration		
J3:IS200TREGH1A	First TREG Board	Connected, not connected
KESTOP1_Fdbk1	Emergency stop - When TREG, ESTOP1, inverse sense, K4 relay, True = Run - board point	Point edit (input BIT)
Contact1	Trip interlock 1 (first of 7) - board point	Point edit (input BIT)
ContactInput	Trip interlock 1 used	Used, unused
TripEnable	Trip interlock active	Enable, disable
TrpTimeDelay	Time delay before tripping turbine after contact opens (seconds)	0 to 10
SeqOfEvents	Record contact transitions in sequence of events	Enable, disable
K1_Fdbk	Trip Relay 1 feedback (first of 3) - board point	Point edit (input BIT)
RelayOutput	Relay feedback used	Used, unused
KE1_Fdbk	Economizer relay for trip solenoid feedback (first of 3) - board point	Point edit (input BIT)
RelayOutput	Economizer relay feedback used	Used, unused
K4CL_Fdbk	Drive Control Valve Servos Closed, use ONLY for Steam Turbine Simplex - board point	Point Edit (Input BIT)
Relay output	Servo valve clamp used	Used, unused
K25A	Synchronizing check relay on TTUR - board point	Point edit (input BIT)
SynchCheck	Synch check relay K25A used	Used, unused

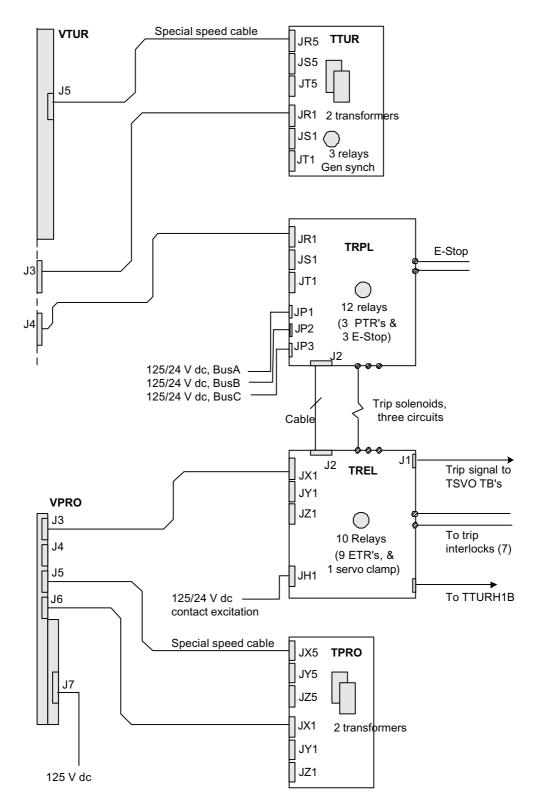
Typical TREG Configuration

SystemFreq	System frequency in Hz	50 or 60
ReferFreq	Select generator frequency reference for PLL, standard PR input or from signal space	PR standard or signal space
TurbRPM	Rated load turbine RPM	0 to 20,000
VoltageDiff	Maximum voltage difference in kV rms for synchronizing	0 to1,000
FreqDiff	Maximum frequency difference in Hz for synchronizing	0 to 0.5
PhaseDiff	Maximum phase difference in degrees for synchronizing	0 to 30
GenVoltage	Minimum generator voltage in kV rms for synchronizing	1 to 1,000
BusVoltage	Minimum bus voltage in kV rms for synchronizing	1 to 1,000
J4A:IS200TREGH1A	Second TREG board	Connected, not connected
KESTOP2_Fdbk	When TREG, ESTOP, inverse sense, K4 relay, True = Run - board point	Point edit (input BIT)
K4_Fdbk	Trip relay 4 feedback (first of three) - board point	Point edit (input BIT)
KE4_Fdbk	Economizing relay for trip solenoid 4 (first of three) - board point	Point edit (input BIT)
Board Points (Signals)	Description - Point Edit (Enter Signal Connnection)	Direction Type
	See point edit names above	

TRPL/TREL Large Steam Turbine Primary and Emergency Trip

TRPL and TREL are used to provide primary and emergency overspeed protection for large steam turbines. These two terminal boards are used in a similar way as TRPG and TREG are used on gas turbine applications.

Up to three trip solenoids can be connected between the TREL and TRPL terminal boards. TREL provides the positive side of the 125 V dc to the solenoids and TRPL provides the negative side. VTUR provides primary overspeed protection and the emergency stop functions. It controls the 12 relays on TRPL, nine of which form three groups of three to vote inputs controlling the three trip solenoids.



Steam Turbine Control and Protection Boards

Features

TRPL is used for TMR applications only. Three separate power buses, PwrA, PwrB, PwrC for solenoid power, are brought in through connectors JP1, JP2, and JP3, and then distributed to TREL through connector J2. In the TREL, three separate power buses, PwrA, PwrB, PwrC for solenoid power, are brought in through connector J2 from TRPL.

The power buses have a nominal voltage of 125 V dc (70 to 145 V dc) or 24 V dc (18 to 32 V dc). The board includes power bus monitoring (three buses). The maximum current per bus is 3 amps.

Each of the three trip solenoids is controlled by three relays using 2/3 contact voting. The relay output rating (for 100,000 operations) is as follows:

- At 24 V dc, 3 A, L/R = 100 milliseconds, with suppression
- At 125 V dc, 1.0 A, L/R = 100 milliseconds, with suppression

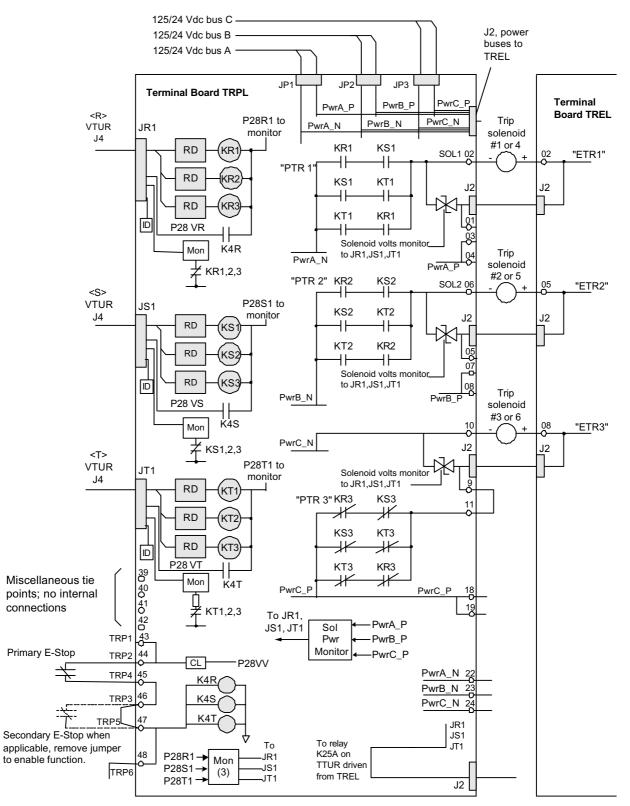
The trip circuits include solenoid suppression, and associated solenoid voltage monitoring and trip relay contact monitoring. In the TRPL, the hardwired trip (E-STOP) and associated monitoring provides approximately 6.6 V dc to VTUR when the K4 relays are picked up. In the TREL, seven dry contact inputs are used as trip interlocks, and the excitation and signal are monitored and fanned to the three VPROs.

Configuration

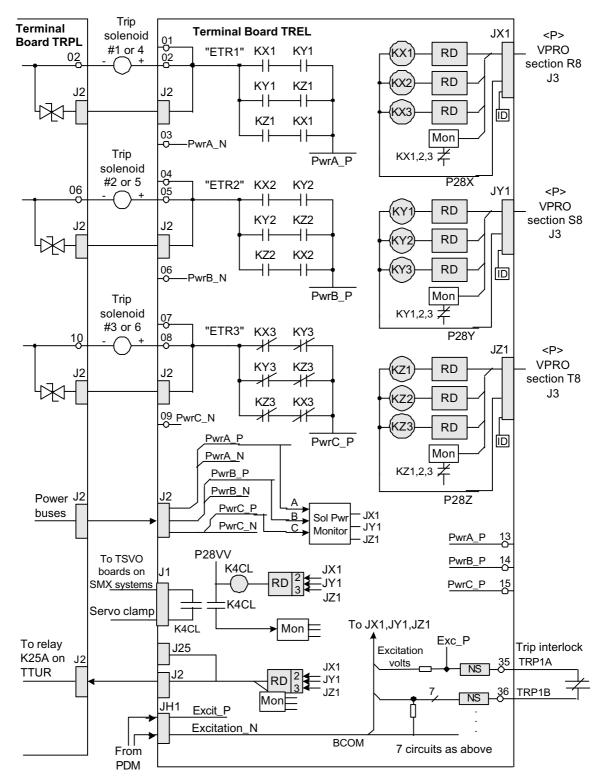
TRPL configuration is similar to TRPG but there are no flame detectors. Only the single-wide VTUR is used with a single J4 connector.

TREL configuration is similar to TREG but there are no emergency stop inputs (KESTOP), and no economizer relay solenoid feedbacks (KE#_Fdbk). Only one TREL can be connected to the VPRO.

The TREL includes the synch check relay driver, K25A, and associated monitoring, the same as on TREG, and the servo clamp relay driver, K4CL, and its associated monitoring.



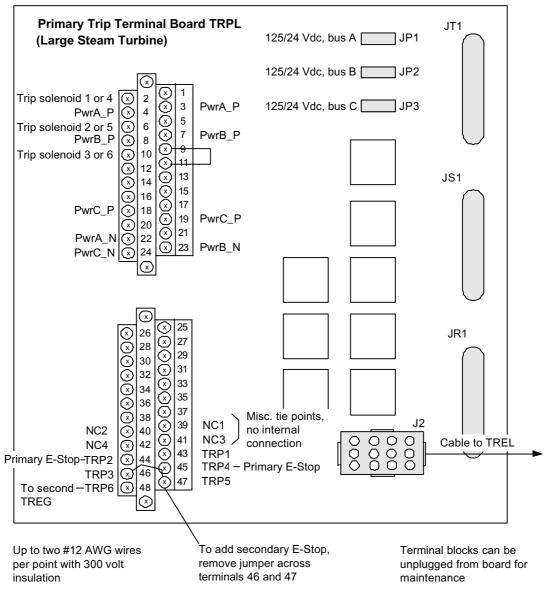
TRPL Terminal Board



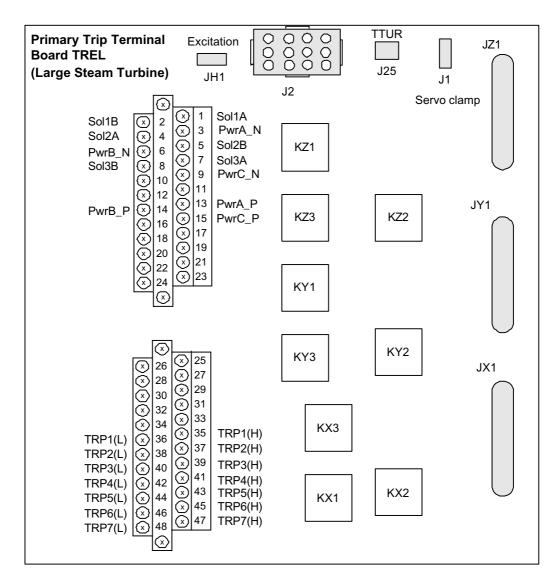
TRPL Terminal Board (continued)

Installation

The three trip solenoids are wired directly to the first I/O terminal block. The primary emergency stop and optional secondary emergency stop are wired to the second terminal block. Trip solenoid power is supplied through plugs JP1, JP2, and JP3. The wiring connections are shown in the following figures.



TRPL Terminal Board Wiring



Up to two #12 AWG wires per point with 300 V insulation

Terminal blocks can be unplugged from terminal board for maintenance

TREL Terminal Board Wiring

TRPS/TRES Small/Medium Steam Turbine Primary Trip

TRPS and TRES are used to provide primary and emergency overspeed protection for small/medium size steam turbines. These two terminal boards are used in a similar way as TRPG and TREG are used on gas turbine applications.

Up to three trip solenoids can be connected between the TRES and TRPS terminal boards. TRES provides the positive side of the 125 V dc to the solenoids and TRPS provides the negative side.

VTUR provides primary overspeed protection and the emergency stop functions. It controls the six relays on TRPS, three of which control the three trip solenoids.

VPRO provides emergency overspeed protection and the trip functions. It controls the three relays on TRES, which control the three trip solenoids.

Features

TRPS and TRES are used for both simplex and TMR applications. Three separate power buses, PwrA, PwrB, PwrC for solenoid power, are brought in the TRPS through connectors JP1, JP2, and JP3, and then distributed to TRES through connector J2.

The power buses have a nominal voltage of 125 V dc (70 to 145 V dc) or 24 V dc (18 to 32 V dc). The board includes power bus monitoring (three buses). The maximum current per bus is 3 amps.

Each of the three trip solenoids is controlled by a relay driver providing 2/3 logic voting with signals from JR1, JS1, and JT1. In the Simplex application, the relay driver is controlled by a single signal from JA1. The relay output rating (for 100,000 operations) is as follows:

- At 24 V dc, 3 A, L/R = 100 milliseconds, with suppression
- At 125 V dc, 1.0 A, L/R = 100 milliseconds, with suppression

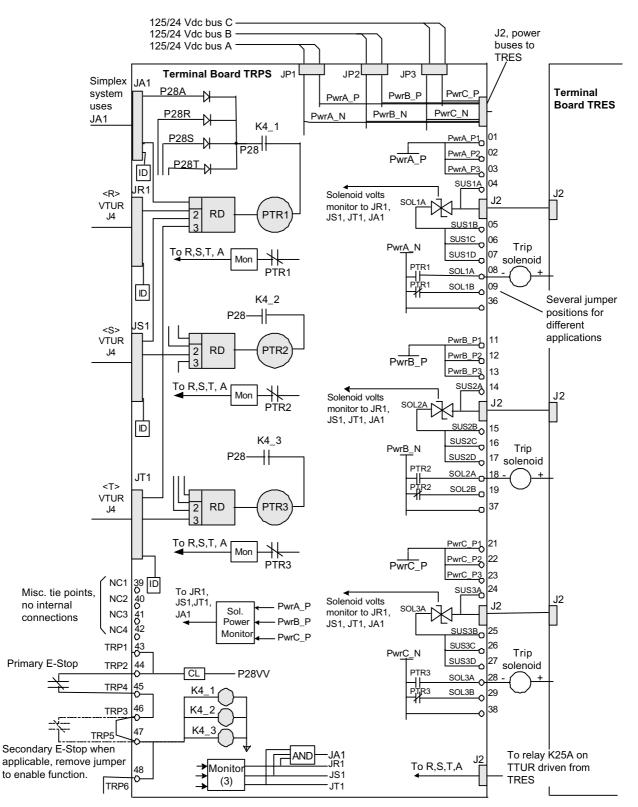
The trip circuits include solenoid suppression, and associated solenoid voltage monitoring and trip relay contact monitoring. In the TRPS, the hardwired trip (E-STOP) and associated monitoring provides approximately 6.6 V dc to VTUR when the K4 relays are picked up.

In the TRES, seven dry contact inputs are used as trip interlocks, and the excitation and signal are monitored and fanned to the three VPROs. The board includes the synch check relay driver, K25A, and associated monitoring, the same as on TREG, and the servo clamp relay driver, K4CL, and its associated monitoring.

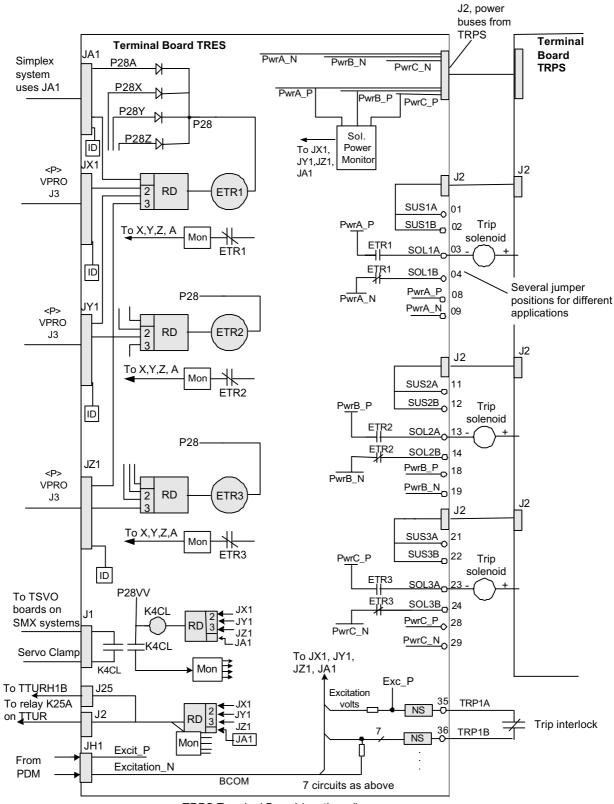
Configuration

TRPS configuration has no flame detectors. Only the single-wide VTUR is used with a single J4 connector.

TRES configuration has no emergency stop, and no economizing relay feedback. Only one VPRO J3 connector is used; there can be no second TRES board.



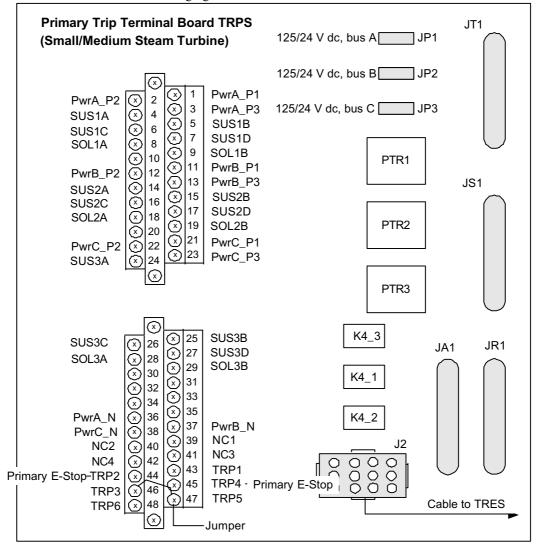
TRPS Terminal Board



TRPS Terminal Board (continued)

Installation

In the TRPS board, three trip solenoids are wired directly to the first and second I/O terminal blocks. The primary emergency stop and optional secondary emergency stop are wired to the second terminal block. Trip solenoid power is supplied throu0gh plugs JP1, JP2, and JP3. The wiring connections are shown in the following figure.

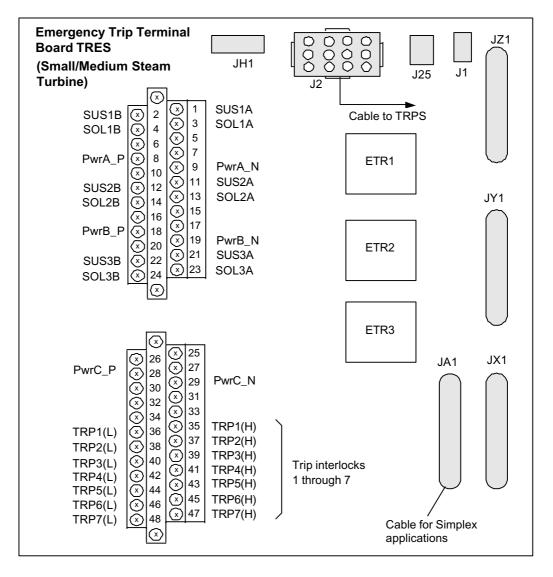


Up to two #12 AWG wires per point with 300 V insulation

Terminal blocks can be unplugged from terminal board for maintenance

TRPS Terminal Board Wiring

In the TRES board, the three trip solenoids are wired directly to the first I/O terminal block. The seven trip interlocks are wired to the second terminal block. Trip solenoid power is supplied through plug J2 from TRPS, and contact excitation comes through JH1 from the PDM. The wiring connections are shown in the following figure.



Up to two #12 AWG wires per point with 300 V insulation

Terminal blocks can be unplugged from terminal board for maintenance

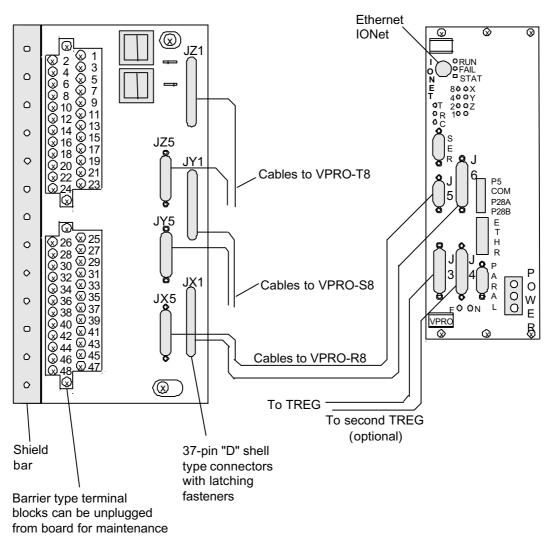
TRES Terminal Board Wiring

TPRO Turbine Protection Terminal Board

The VPRO) and associated terminal board (TPRO) provide an independent emergency overspeed protection system. The protection system consists of triple redundant VPRO boards in a module separate from the turbine control system, controlling the trip solenoids through TREG.

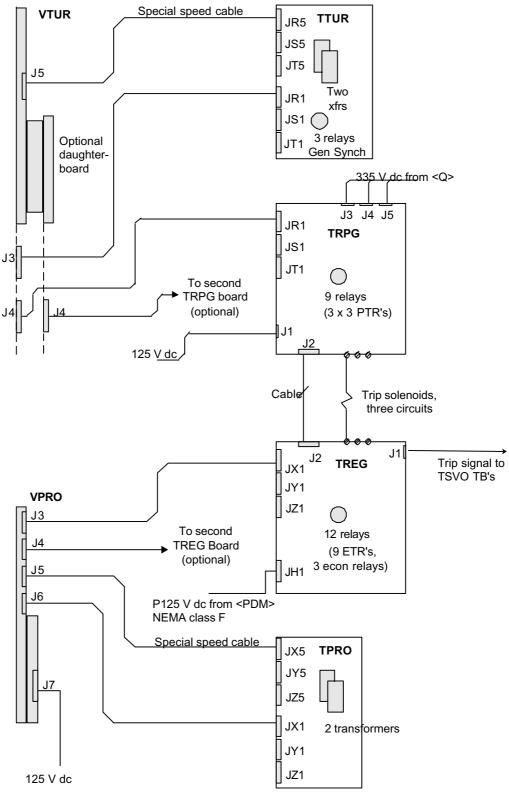
TPRO Terminal Board

VPRO-R8

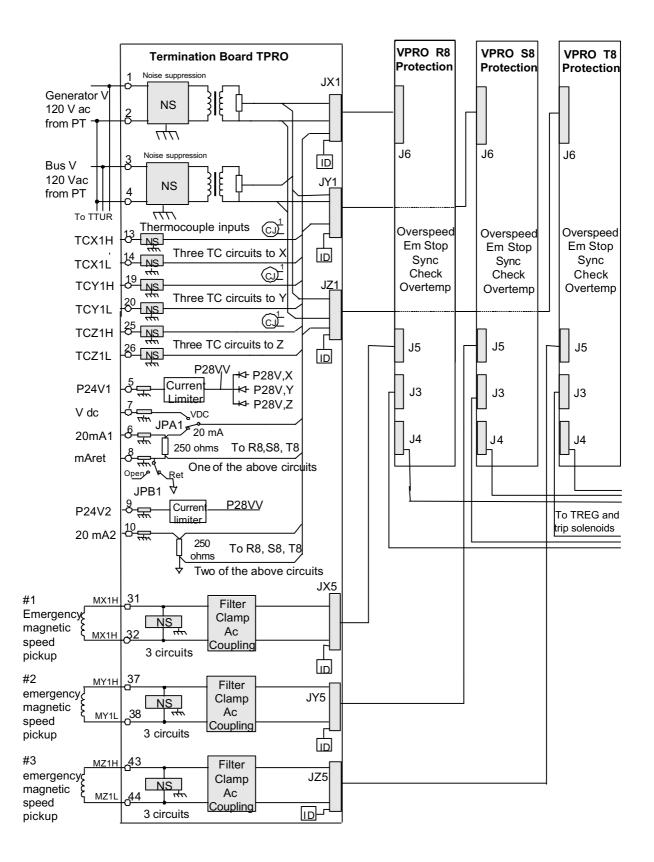


Turbine Protection Terminal Board, VPRO Board, and Cabling

The following figure shows how the VTUR and VPRO processor boards share in the turbine protection scheme. Either one can independently trip the turbine through the relays on TRPG or TREG.

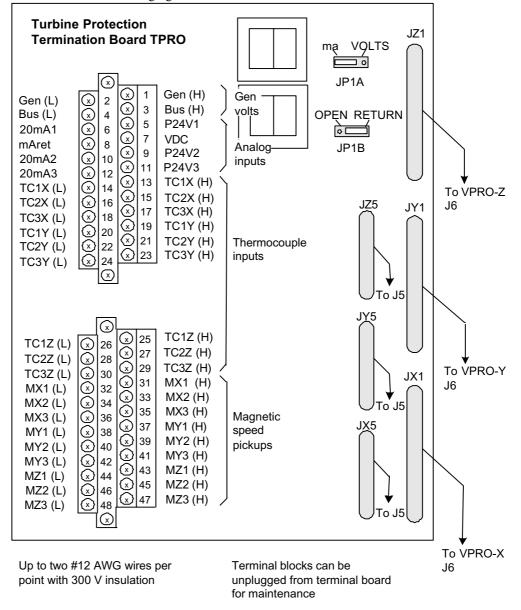


Turbine Control and Protection Boards



Installation

The generator and bus potential transformers and the analog inputs are wired to the first TPRO terminal block. The magnetic speed pickups are wired to the second block. Jumpers JP1A and JP1B are set to give either a 4–20 mA or voltage input on the first of the three analog inputs. The wiring connections are shown in the following figure.



Terminal Board TPRO

Operation

The main purpose of the <P> protection module is emergency overspeed (EOS) protection for the turbine. In addition, the module has backup synchronization check protection, three analog current inputs, and nine thermocouple inputs, primarily intended for exhaust overtemperature protection on gas turbines.

The protection module is always triple redundant with three completely separate and independent sections named X, Y, and Z. Any one of these sections can be powered down and replaced while the turbine is running without jeopardizing the protection system. Each section contains its own I/O interface, processor, power supply, and Ethernet communications (IONet) to the control modules. The communications allow initiation of test commands from the control module to the protection module and the monitoring of EOS system diagnostics in the control module and on the operator interface. Communications are resident on the VPRO board which is the heart of the system.

Features

Speed Control and Overspeed Protection

Speed control and overspeed protection is implemented with six passive, magnetic speed pickups. The first three are monitored by the control module(s) which use the median signal for speed control and the primary overspeed protection. The second three are separately connected to the X, Y, and Z sections of the protection module. Provision is made for nine passive magnetic speed pickups or active pulse rate transducers (TTL type) on the TPRO terminal board with three being monitored by each of the X, Y, and Z sections. Separate overspeed trip settings are programmed into the application software for the primary and emergency overspeed trip limits, and a second emergency overspeed trip limit must be programmed into the I/O configurator to confirm the EOS trip point.

The speed is calculated by counting passing teeth on the wheel and measuring the time involved. Another protection feature is the calculation of the rate of change of speed which is compared with 100%/sec and transmitted to the control module to trip the unit if it is detected after the turbine reaches a predetermined steady-state speed. This steady-state speed limit is a tuning constant located in the controller's application software. Another speed threshold which is monitored by the EOS system is 10% speed. This is transmitted to the control module to verify that there is no gross disagreement between the first set of three speed pickups being monitored by the controller (for speed control and the primary overspeed protection) and the second set of three speed pickups being monitored by the EOS system.

Interface To Trip Solenoids

The trip system combines the primary trip interface from the control module(s) with the EOS trip interface from the protection module. Three separate, triple redundant trip solenoids (also called electrical trip devices - ETDs) are used to interface with the hydraulics. The ETDs are connected between the TRPG and TREG terminal boards. A separately fused 125 V dc feeder is provided from the turbine control for each solenoid which energize in the run mode and de-energize in the trip mode.

The VPRO board has a VME interface to allow programming and testing in a VME rack; however, the backplane is neutralized when plugged into the protection module to eliminate any continuity between the three independent sections.

Backup Synch Check Protection

Backup synch check protection is provided in the $\langle P \rangle$ protection module. The generator and bus voltages are supplied from two, single phase, potential transformers (PTs) secondary output supplying a nominal 115 V rms. The maximum cable length between the PTs and the turbine control is 100 meters of 18 AWG twisted, shielded wire. Each PT is magnetically isolated with a 1,500 V rms rated barrier and a circuit load less than 3 VA. The synch algorithms are based on phase lock loop techniques. Phase error between the generator and bus voltages is less than +/-1 degree at nominal voltage and 50/60 Hz. A frequency range of 45 to 66 Hz is supported with the measured frequency within 0.05% of the input frequency. The algorithm is illustrated under TTUR, generator synchronizing.

Each PT input is internally connected in parallel to the X, Y, and Z sections of the Protection Module. The triple redundant phase slip windows result in a voted logical output on the TREG terminal board which drives the K25A relay. This relay's contacts are connected in series with the synch permissive relay (K25P) and the auto synch relay (K25) to insure that no false command is issued to close the generator breaker. Similarly, contacts from the K25A contact are connected in series with the contacts from remote, manual synchronizing equipment to insure no false commands.

Thermocouple and Analog Inputs

Thermocouple and analog inputs are available in the protection module, primarily for gas turbine applications. Nine thermocouple inputs are monitored with three connected to each section of the protection module. These are generally used for backup exhaust overtemperature protection. Also, one \pm 5, 10 V dc, 4–20 mA (selectable) input, and two 4–20 mA inputs can be connected to the TPRO terminal board which feeds the inputs in parallel to the three sections of the protection module.

Power Supply

Each VPRO board has its own on-board power supply. This generates 5 V dc and 28 V dc using 125 V dc supplied from the cabinet PDM. The entire TMR VPRO module therefore has three power supplies for high reliability.

Specifications

VPRO Board Specifications

Item	Specificati	ion
Number of inputs	TPRO:9	Passive speed pickups 1 Generator and 1 bus voltage 9 Thermocouples 1 4–20 mA current or voltage 2 4–20 mA current
	VPRO: 3	 Passive speed pickups Generator and 1 bus voltage Thermocouples 4–20 mA current or voltage 4–20 mA current Trip interlocks Emergency stop

Number of Outputs	TREG:3	 Trip solenoids per TREG 3 Economizer relays 1 Breaker relay command, K25A on TTUR 1 Servo clamp relay contact, to TSVO boards
	VPRO:6	Trip solenoids 6 Economizer relays 1 Breaker relay command, K25A on TTUR 1 Servo clamp relay contact, to TSVO boards
Power Supply Voltage	TPRO: 28 V (dc from X, Y, and Z boards, voted
	VPRO: Input	supply 125 V dc (70–145 V dc) Output 5 V dc and 28 V dc
Frame Rate	Up to 100 Hz	Ζ
MPU Characteristics	Output gene block, with in The maximu The system a	tance 200 ohms with inductance of 85 mH. rates 150 V p-p into 60k ohms at the TPRO terminal isufficient energy for a spark. m short circuit current is approximately 100 mA. applies up to 400 ohm normal mode load to the input uce the voltage at the terminals.
MPU Cable	that shielded	be up to 300 m (984 ft) from the cabinet, assuming I pair cable is used, with typical 70 nF single ended or ntial capacitance, and 15 ohms resistance.
MPU Pulse Rate Range	2 Hz to 20 kł	Hz
MPU Pulse Rate Accuracy	Noise of the	ding; resolution is 15 bits at 100 Hz acceleration measurement is less than \pm 50 Hz/sec Hz signal being read at 10 ms.
MPU Input Circuit Sensitivity		nal is 27 mV pk at 2 Hz nal is 450 mV pk at 14 kHz
Generator and Bus Voltage Sensors	Voltage accu Frequency a Phase differe Allowable vo	hase potential transformers, 115 V rms secondary uracy is 0.5% of rated V rms ccuracy 0.05% ence measurement better than 1 degree. Itage range for synchronizing is 75 to 130 V rms. as a load of less than 3 VA.
Thermocouple Inputs	Same specifi	ications as for VTCC board
Analog Inputs	Same specifi	cations as for VAIC board

Diagnostics

Board diagnostics cover the thermocouple limits, reference voltage, cold junction, analog input health, and contact input test failure. Relay diagnostics cover the trip relay driver and contact feedbacks, solenoid voltage, economizer relay driver and contact feedbacks, K25A relay driver and coil, and the servo clamp relay driver and contact feedback. Voltage diagnostics cover the solenoid power bus, and the voltage to the solenoids.

Connectors JX1, JY1, JZ1, JX5, JY5, and JZ5 on the terminal board have their own ID device, which is interrogated by the I/O board. The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and the plug location.

Configuration

Typical VPRO-TPRO Configuration

Parameter	Description	Choices
Configuration		
Turbine_Type	Define the type of turbine from selection of ten types	Two gas turbine Two LM Two large steam One medium steam One small steam Two stage GT
LMTripZEnable	On LM machine, when no PR on Z, enable vote for trip	Enable, disable
OT_Trip_Enbl	Enable overtemperature trip	Enable, disable
OvrTemp_Trip	Iso-thermal overtemperature trip setting for exhaust thermocouples in degree F	-60 to 2,000
CPD_Corner	Overtemperature trip compressor discharge pressure in psi at which CDP bias starts	0 to 450
CPD_Slope	Overtemperature trip compressor discharge pressure bias slope in degrees F/psi	-10 to 0
TA_Trip_Enab1	Steam, enable trip anticipation on ETR1	Enable, disable
RatedRPM_TA	Steam, rated RPM, used for trip anticipation calculation	0 to 20,000
Auto Reset	Automatic restoring of thermocouples removed from scan	Enable, disable
DiagSolPwrA	When using TREL/TRES, solenoid power, BusA, diagnostic enable	Enable, disable
Min_MA_Input	Minimum mA for healthy 4–20 mA Input	0 to 21
Max_MA_Input	Maximum mA for healthy 4–20 mA Input	0 to 21
AccelCalType	Select acceleration calculation type	Slow, medium, fast
J5:IS200TPROH1A	J5 cable section of TPRO board	
PulseRate1	First of three speed inputs - board point	Point edit (input FLOAT)
PRType	Selects gearing (resolution)	Unused, PR<6,000 Hz, PR>6,000 Hz
PRScale	Pulses per revolution (output RPM)	0 to 1,000
OS_Setpoint	Overspeed trip setpoint in RPM	0 to 20,000
OS_Tst_Delta	Offline overspeed test setpoint delta in RPM	-2,000 to 2,000
Zero_Speed	Zero speed for this shaft in RPM	0 to 20,000
Min_Speed	Minimum speed for this shaft in RPM	0 to 20,000
Accel_Trip	Enable Acceleration trip	Enable, disable
Acc-Setpoint	Accelerate trip setpoint in RPM/second	0 to 20,000
TMR_DiffLimt	Difference limit for voted pulse rate inputs in engineering units	0 to 20,000
J6:IS200TPROH1A	J6 cable section of TPRO board	

BusPT_KVolts	kV rms, bus potential transformer - board point	Point edit (input FLC	DAT)
PT_Input	PT input in kV rms for PT_Output	0 to 1,000	
PT_Output	PT output in V rms for PT_Input-typically 115	60 to 150	
TMR_DiffLimt	Difference limit for voted PT inputs in %	0 to 100	
GenPT_KVolts	kV rms, generator PT, configuration similar to bus PT - board point	Point edit (input FLC	DAT)
TC11	Thermocouple 1, for X module (first of 3) - board point	Point edit (input FLC	DAT)
ThermCpIType	Select thermocouple type or mV input	Unused, mV, T, K, J,	E
Low pass filter	Enable 2 Hz low pass filter	Enable, disable	
TC21	Thermocouple 1, for Y module (first of three) configure as above - board point	Point edit (input FLC	DAT)
TC31	Thermocouple 1, for Z module (first of three) configure as above - board point	Point edit (input FLC	DAT)
Cold Junction	CJ for thermocouples 1-3	Point edit (input FLC	DAT)
TMR_DiffLimt	Difference limit for voted TMR CJ inputs in degrees F	-60 to 2,000	
AnalogIn1	First of three analog inputs - board point	Point edit (input FLC	DAT)
Input Type	Type of analog input	Unused, 4–20 mA, \pm	10 V
Low_Input	Input mA at low value	-10 to 20	
Low_Value	Input value in engineering units at low value	-3.402e+38 to 3.402	e+38
High_Input	Input mA at high value	-10 to 20	
High_Value	Input value in engineering units at high mA	-3.402e+38 to 3.402e+38	
InputFilter	Filter bandwidth in Hz	Unused, 12 Hz, 6 Hz Hz, 0.75 Hz	, 3Hz, 1.5
Trip_Enable	Enable trip for this mA Input	Enable, disable	
TripSetpoint	Trip setpoint in engineering units	-3.402e+38 to 3.402	e+38
TripTimeDelay	Time delay before tripping turbine after signal exceeds setpoint in seconds	0 to 10	
TMR_DiffLimt	Difference limit for voted TMR inputs in % of (High_Value-Low_Value)	0 to 100	
J3:IS200TREGH1A	First TREG board (see TREG section for configuration)	Connected, not conn	ected
J4:IS200TREGH1A	Second TREG board (optional)	Connected, not conn	ected
Board Points (Signals)	Description - Point Edit (Enter Signal Connection)	Direction	Туре
L3DIAG-VPRO1	Board diagnostic	Input	BIT
L3DIAG-VPRO2	Board diagnostic	Input	BIT
L3DIAG-VPRO3	Board diagnostic	Input	BIT
PR1_Zero	L14HP_ZE	Input	BIT
PR2_Zero	L14IP_ZE	Input	BIT
PR3_Zero	L14LP_ZE	Input	BIT
Spare	Spare	Input	BIT
OS1_Trip	L12HP_TP	Input	BIT

OS2_Trip	L12IP_TP	Input	BIT
OS3_Trip	L12LP_TP	Input	BIT
Dec1_Trip	L12HP_DEC	Input	BIT
Dec2_Trip	L12IP_DEC	Input	BIT
Dec3_Trip	L12LP_DEC	Input	BIT
Acc1_Trip	L12HP_ACC	Input	BIT
Acc2_Trip	L12IP_ACC	Input	BIT
Acc3_Trip	L12LP_ACC	Input	BIT
TA_Trip	Trip anticipate trip L12TA_TP	Input	BIT
TA_StpLoss	L30TA	Input	BIT
OT_Trip	L26TRP	Input	BIT
MA1_Trip	L3MA_TRP1	Input	BIT
MA2_Trip	L3MA_TRP2	Input	BIT
MA3_Trip	L3MA_TRP3	Input	BIT
SOL1_Vfdbk	When TREG, trip solenoid 1 voltage	Input	BIT
:	:	Input	BIT
SOL6_Vfdbk	When TREG, trip solenoid 6 voltage	Input	BIT
L25A_Cmd	L25A breaker close pulse	Input	BIT
Cont1_TrEnab	Configure - Contact 1 trip enabled	Input	BIT
:	:	Input	BIT
Cont7_TrEnab	Configure - Contact 7 trip enabled	Input	BIT
Acc1_TrEnab	Configure - Accelerate 1 trip enabled	Input	BIT
:	:	Input	BIT
Acc3_TrEnab	Configure - Accelerate 3 trip enabled	Input	BIT
OT-TrEnab	Configure - Overtemperature trip enabled	Input	BIT
GT_1Shaft	Configure - Gas turbine, 1 shaft enabled	Input	BIT
GT_2Shaft	Configure - Gas turbine, 2 shaft enabled	Input	BIT
LM_2Shaft	Configure - LM turbine, 2 shaft enabled	Input	BIT
LM_3Shaft	Configure - LM turbine, 3 shaft enabled	Input	BIT
LargeSteam	Configure - Large steam 1, enabled	Input	BIT
MediumSteam	Configure - Medium steam, enabled	Input	BIT
SmallSteam	Configure - Small steam, enabled	Input	BIT
STag_GT_1S	Configure - Stage 1 shaft, enabled	Input	BIT
STag_GT_2S	Configure - Stage 2 shaft, enabled	Input	BIT
ETR1_Enab	Configure - ETR1 relay enabled	Input	BIT
:	:	Input	BIT
ETR6_Enab	Configure - ETR6 relay enabled	Input	BIT
K4CL_Enab	Configure - Servo clamp relay enabled	Input	BIT
K25A_Enab	Configure - Sync check relay enabled	Input	BIT
	g		

LSCFG1_TripHP configure tripInputBITLSCFG2_TripIP configure tripInputBITLSCFG3_TripLP configure tripInputBITOS1_SP_CfgErIP overspeed setpoint configure mismatch errorInputBITOS2_SP_CfgErIP overspeed setpoint configure mismatch errorInputBITComposTrip1Composite trip 1InputBITComposTrip2Composite trip 3InputBITLSESTOP1ESTOP 1 trip, TREG, J3InputBITLSESTOP1ESTOP 2 trip, TREG, J4InputBITLSESTOP1ESTOP 2 trip, TREG, J4InputBITLSCont1_TripContact 7 tripInputBITLSCont7_TripContact 7 tripInputBITLSCont7_TripContact 7 tripInputBITBus FreqSFL 2 HzInputBITGenFreqSFL 2 HzInputFLOATGenFreq 0ffSFDIFF2 slip Hz - generator low is negativeInputFLOATGenFreqDiffSSDIFF2 slip Hz - generator lag is negativeInputFLOATPR1_AccelHP accelerate in RPM/secondInputFLOATPR2_AccelLP accelerate in RPM/secondInputFLOATPR3_AccelLP accelerate in RPM/secondInputFLOATPR3_MaxLP maximum speed since last zero speed in RPMInputFLOATPR3_MaxLP maximum speed since last zero speed in RPMInputFLOATPR3_MaxLP maximum speed since last zero speed in RPMInput				
L5CFG3_Trip LP configure trip Input BIT OS1_SP_CfgEr HP overspeed setpoint configure mismatch error Input BIT OS2_SP_CfgEr LP overspeed setpoint configure mismatch error Input BIT OS3_SP_CfgEr LP overspeed setpoint configure mismatch error Input BIT ComposTrip1 Composite trip 2 Input BIT ComposTrip2 Composite trip 2 Input BIT L5ESTOP1 ESTOP 2 trip, TREG, J3 Input BIT L5ESTOP2 ESTOP 2 trip, TREG, J4 Input BIT L5Cont1_Trip Contact 7 trip Input BIT L5Cont7_Trip Contact 7 trip Input BIT L9StaftLock LP shaft locked Input BIT Bus Freq SF 2 Hz Input FLOAT GenFreq0 SF 2 Hz Input FLOAT GenVoltsDiff DV_ERR kV rms - generator low is negative Input FLOAT GenFreq0iff SFDIFF2 shape degrees - generator lag is negative Input FLOAT PR1_Accel HP accelerate in RPM/second Input FLOAT <	L5CFG1_Trip	HP configure trip	Input	BIT
OS1_SP_CfgErHP overspeed setpoint configure mismatch errorInputBITOS2_SP_CfgErIP overspeed setpoint configure mismatch errorInputBITOS3_SP_CfgErLP overspeed setpoint configure mismatch errorInputBITComposTrip1Composite trip 1InputBITComposTrip2Composite trip 2InputBITComposTrip3Composite trip 3InputBITL5ESTOP1ESTOP 1 trip, TREG, J3InputBITL5ESTOP2ESTOP 2 trip, TREG, J4InputBITL5Cont1_TripContact 1 tripInputBITL5Cont7_TripContact 7 tripInputBITL5Cont7_TripContact 7 tripInputBITL6Cont7_TripContact 7 tripInputBITGenFreqSF 2 HzInputFLOATGenFreqSF 2 HzInputFLOATGenPhaseDiffSFDIFF2 slip Hz - generator low is negativeInputFLOATPR1_AccelHP accelerate in RPM/secondInputFLOATPR3_AccelLP accelerate in RPM/secondInputFLOATPR3_AccelLP maximum speed since last zero speed in RPMInputFLOATPR3_MaxLP maximum speed since last zero speed in RPMInputFLOATPR4_Max<	L5CFG2_Trip	IP configure trip	Input	BIT
OS2_SP_CfgEr IP overspeed setpoint configure mismatch error Input BIT OS3_SP_CfgEr LP overspeed setpoint configure mismatch error Input BIT ComposTrip1 Composite trip 1 Input BIT ComposTrip2 Composite trip 2 Input BIT ComposTrip3 Composite trip 3 Input BIT LSESTOP1 ESTOP 1 trip. TREG, J3 Input BIT LSESTOP2 ESTOP 2 trip. TREG, J4 Input BIT LSCont1_Trip Contact 1 trip Input BIT LSCont7_Trip Contact 7 trip Input BIT LPShaftLock LP shaftLocked Input BIT Bus Freq SFL 2 Hz Input FLOAT GenFreq SFL 2 Hz Input FLOAT GenPhaseDiff SDIFF2 slip Hz - generator low is negative Input FLOAT PR1_Accel IP accelerate in RPM/second Input FLOAT PR2_Accel IP accelerate in RPM/second Input FLOAT PR3_Accel LP accelerate in RPM/second Input FLOAT PR3_Max <	L5CFG3_Trip	LP configure trip	Input	BIT
OS3_SP_CfgErLP overspeed setpoint configure mismatch errorInputBITComposTrip1Composite trip 1InputBITComposTrip2Composite trip 2InputBITComposTrip3Composite trip 3InputBITL5ESTOP1ESTOP 2 trip, TREG, J3InputBITL5ESTOP2ESTOP 2 trip, TREG, J4InputBITL5Cont7_TripContact 1 tripInputBITL5Cont7_TripContact 7 tripInputBITL9ShaftLockLP shaft lockedInputBITBus FreqSF 2 HzInputFLOATGen VolsDiffDV_ERR kV rms - generator low is negativeInputFLOATGen VolsDiffSDIFF2 shase degrees - generator lag is negativeInputFLOATGenPreqDiffSSDIFF2 phase degrees - generator lag is negativeInputFLOATPR1_AccelHP accelerate in RPM/secondInputFLOATPR1_AccelLP accelerate in RPM/secondInputFLOATPR3_AccelLP maximum speed since last zero speed in RPMInputFLOATPR3_MaxLP maximum speed since last zero speed in RPMInputFLOATPR3_MaxLP maximum speed since last zero speed in RPMInputFLOATSynCk_PermL25A_PERM - sync check permissiveOutputBITOnLineOS1XtL97HP_TST1 - online HP overspeed testOutputBITOnLineOS1XtL97HP_TST2 - online HP overspeed testOutputBITOnLineOS1XtL97HP_TST2 - online HP overspeed test	OS1_SP_CfgEr	HP overspeed setpoint configure mismatch error	Input	BIT
ComposTrip1 Composite trip 1 Input BIT ComposTrip2 Composite trip 2 Input BIT ComposTrip3 Composite trip 3 Input BIT L5ESTOP1 ESTOP 1 trip, TREG, J3 Input BIT L5ESTOP2 ESTOP 2 trip, TREG, J4 Input BIT L5Cont1_Trip Contact 1 trip Input BIT L5Cont7_Trip Contact 7 trip Input BIT L9StaftLock LP shaft locked Input BIT Bus Freq SFL 2 Hz Input FLOAT GenFreq Off DV_ERR kV rms - generator low is negative Input FLOAT GenPhaseDiff SDIFF2 phase degrees - generator lag is negative Input FLOAT PR1_Accel HP accelerate in RPM/second Input FLOAT PR3_Accel LP accelerate in RPM/second Input FLOAT PR3_Max LP maximum speed since last zero speed in RPM Input FLOAT PR3_Max LP maximum speed since last zero speed in RPM Input FLOAT P	OS2_SP_CfgEr	IP overspeed setpoint configure mismatch error	Input	BIT
ComposTrip2Composite trip 2InputBITComposTrip3Composite trip 3InputBITL5ESTOP1ESTOP 1 trip, TREG, J3InputBITL5ESTOP2ESTOP 2 trip, TREG, J4InputBITL5Cont1_TripContact 1 tripInputBITL5Cont1_TripContact 1 tripInputBITL5Cont1_TripContact 7 tripInputBITL5Cont7_TripContact 7 tripInputBITBus FreqSFL 2 HzInputFLOATGenFreqSF 2 HzInputFLOATGenFreqDiffSFDIFF2 slip Hz, generator low is negativeInputFLOATGenFreqDiffSFDIFF2 slip Hz, generator slow is negativeInputFLOATPR1_AccelHP accelerate in RPM/secondInputFLOATPR2_AccelIP accelerate in RPM/secondInputFLOATPR3_AccelLP accelerate in RPM/secondInputFLOATPR4_MaxHP maximum speed since last zero speed in RPMInputFLOATPR2_MaxL25A_PERM - sync check permissiveOutputBITSynCk_PermL25A_PERM - sync check papassOutputBITOnLineOS1TstL97H_TST1 - online HP overspeed testOutputBITOnLineOS1TstL97H_TST1 - online HP overspeed testOutputBITOffLineOS3TstL97L_TST2 - offline IP overspeed testOutputBITOffLineOS3TstL97L_TST2 - offline IP overspeed testOutputBITOffLineOS3TstL97L_TST2 - offline IP overspe	OS3_SP_CfgEr	LP overspeed setpoint configure mismatch error	Input	BIT
ComposTrip3Composite trip 3InputBITL5ESTOP1ESTOP 1 trip, TREG, J3InputBITL5ESTOP2ESTOP 2 trip, TREG, J4InputBITL5Cont1_TripContact 1 tripInputBIT:::InputBITESTOP 2 trip, TREG, J4InputBITL5Cont1_TripContact 1 tripInputBITL5Cont7_TripContact 7 tripInputBITL9ShaftLockLP shaft lockedInputBITBus FreqSFL 2 HzInputFLOATGenFreqSF 2 HzInputFLOATGenFreqDiffSFDIFF2 slip Hz - generator low is negativeInputFLOATGenPhaseDiffSSDIFF2 phase degrees - generator lag is negativeInputFLOATPR1_AccelHP accelerate in RPM/secondInputFLOATPR2_AccelLP accelerate in RPM/secondInputFLOATPR1_MaxHP maximum speed since last zero speed in RPMInputFLOATPR3_MaxLP maximum speed since last zero speed in RPMInputFLOATPR3_MaxLP maximum speed since last zero speed in RPMInputFLOATSynCk_ByPassL25A_PERM - sync check bypassOutputBITOnLineOS1TstL97HP_TST1 - online HP overspeed testOutputBITOnLineOS1TstL97HP_TST2 - online HP overspeed testOutputBITOffLineOS2TstL97LP_TST2 - online HP overspeed testOutputBITOffLineOS1TstL97LP_TST2 - online HP overspeed test	ComposTrip1	Composite trip 1	Input	BIT
L5ESTOP1ESTOP 1 trip, TREG, J3InputBITL5ESTOP2ESTOP 2 trip, TREG, J4InputBITL5Cont1_TripContact 1 tripInputBIT::InputBITL5Cont7_TripContact 7 tripInputBITLPShaftLockLP shaft lockedInputBITBus FreqSF L 2 HzInputFLOATGenFreqSF 2 HzInputFLOATGenFreqDiffDV_ERR kV rms - generator low is negativeInputFLOATGenFreqDiffSDIFF2 slip Hz - generator slow is negativeInputFLOATGenPhaseDiffSDIFF2 phase degrees - generator lag is negativeInputFLOATPR1_AccelHP accelerate in RPM/secondInputFLOATPR3_AccelLP accelerate in RPM/secondInputFLOATPR1_MaxHP maximum speed since last zero speed in RPMInputFLOATPR2_MaxIP maximum speed since last zero speed in RPMInputFLOATPR3_MaxLP maximum speed since last zero speed in RPMInputFLOATPR3_MaxLP maximum speed since last zero speed in RPMInputFLOATSynCk_BPassL25A_PERM - sync check permissiveOutputBITOnLineOS1TstL97HP_TST1 - online HP overspeed testOutputBITOnLineOS2TstL97HP_TST1 - online HP overspeed testOutputBITOffLineOS2TstL97HP_TST2 - offline IP overspeed testOutputBITOffLineOS3TstL97HP_TST2 - offline IP overspeed testOutput<	ComposTrip2	Composite trip 2	Input	BIT
L5ESTOP2ESTOP 2 trip, TREG, J4InputBITL5Cont1_TripContact 1 tripInputBIT::InputBITL5Cont7_TripContact 7 tripInputBITLPShaftLockLP shaft lockedInputBITBus FreqSFL 2 HzInputFLOATGenFreqSF 2 HzInputFLOATGenVoltsDiffDV_ERR kV rms - generator low is negativeInputFLOATGenPhaseDiffSSDIFF2 phase degrees - generator lag is negativeInputFLOATPR1_AccelHP accelerate in RPM/secondInputFLOATPR2_AccelIP accelerate in RPM/secondInputFLOATPR3_AccelLP accelerate in RPM/secondInputFLOATPR4_MaxHP maximum speed since last zero speed in RPMInputFLOATPR3_MaxLP maximum speed since last zero speed in RPMInputFLOATPR3_MaxLP maximum speed since last zero speed in RPMInputFLOATSynCk_ByPassL25A_PERM - sync check permissiveOutputBITSynCk_ByPassL25A_DERM - sync check bypassOutputBITOnLineOS1TstL97HP_TST1 - online HP overspeed testOutputBITOnLineOS1TstL97LP_TST1 - online HP overspeed testOutputBITOffLineOS1TstL97LP_TST2 - online HP overspeed testOutputBITOffLineOS1TstL97LP_TST2 - online HP overspeed testOutputBITOffLineOS3TstL97LP_TST2 - online HP overspeed testOutputBIT <td>ComposTrip3</td> <td>Composite trip 3</td> <td>Input</td> <td>BIT</td>	ComposTrip3	Composite trip 3	Input	BIT
L5Cont1_TripContact 1 tripInputBIT::InputBITL5Cont7_TripContact 7 tripInputBITLPShaftLockLP shaft lockedInputBITBus FreqSFL 2 HzInputFLOATGenFreqSF 2 HzInputFLOATGen VoltsDiffDV_ERR kV rms - generator low is negativeInputFLOATGenPhaseDiffSFDIFF2 slip Hz - generator slow is negativeInputFLOATGenPhaseDiffSSDIFF2 phase degrees - generator lag is negativeInputFLOATPR1_AccelHP accelerate in RPM/secondInputFLOATPR3_AccelLP accelerate in RPM/secondInputFLOATPR3_AccelLP accelerate in RPM/secondInputFLOATPR3_MaxLP maximum speed since last zero speed in RPMInputFLOATPR3_MaxLP maximum speed since last zero speed in RPMInputFLOATSynCk_PermL25A_PERM - sync check permissiveOutputBITSynCk_ByPassL25A_PERM - sync check bypassOutputBITOnLineOS1TstL97HP_TST1 - online HP overspeed testOutputBITOnLineOS1TstL97HP_TST2 - online HP overspeed testOutputBITOffLineOS2TstL97HP_TST2 - online HP overspeed testOutputBITOffLineOS1TstL97HP_TST2 - online HP overspeed testOutputBITOffLineOS1TstL97HP_TST2 - online HP overspeed testOutputBITOffLineOS2TstL97HP_TST2 - online HP overspeed test<	L5ESTOP1	ESTOP 1 trip, TREG, J3	Input	BIT
: : : Input BIT L5Cont7_Trip Contact 7 trip Input BIT LPShaftLock LP shaft locked Input BIT Bus Freq SFL 2 Hz Input FLOAT GenFreq SF 2 Hz Input FLOAT GenVoltsDiff DV_ERR kV rms - generator low is negative Input FLOAT GenFreqDiff SFDIFF2 slip Hz - generator slow is negative Input FLOAT GenPhaseDiff SSDIFF2 phase degrees - generator lag is negative Input FLOAT PR1_Accel HP accelerate in RPM/second Input FLOAT PR2_Accel IP accelerate in RPM/second Input FLOAT PR3_Accel LP accelerate in RPM/second Input FLOAT PR1_Max HP maximum speed since last zero speed in RPM Input FLOAT PR3_Max LP maximum speed since last zero speed in RPM Input FLOAT SynCk_BYPass L25A_BYPASS - sync check permissive Output BIT SynCk_ByPass L25A_BYPASS - sync check bypass Output BIT OnLineOS1Tst L97HP_TST1 - online HP overspeed test Output BIT OnLineOS1Tst L97HP_TST1 - online HP overspeed test Output BIT OnLineOS1Tst L97HP_TST2 - online HP overspeed test Output BIT OffLineOS1Tst L97HP_TST2 - online HP overspeed test Output BIT OffLineOS3Tst L97HP_TST2 - online HP overspeed test Output	L5ESTOP2	ESTOP 2 trip, TREG, J4	Input	BIT
LSCont7_TripContact 7 tripInputBITLPShaftLockLP shaft lockedInputBITBus FreqSFL 2 HzInputFLOATGenFreqSF 2 HzInputFLOATGenFreqDiffDV_ERR kV rms - generator low is negativeInputFLOATGenPhaseDiffSFDIFF2 slip Hz - generator slow is negativeInputFLOATGenPhaseDiffSSDIFF2 phase degrees - generator lag is negativeInputFLOATPR1_AccelHP accelerate in RPM/secondInputFLOATPR2_AccelIP accelerate in RPM/secondInputFLOATPR3_AccelLP accelerate in RPM/secondInputFLOATPR1_MaxHP maximum speed since last zero speed in RPMInputFLOATPR2_MaxIP maximum speed since last zero speed in RPMInputFLOATPR3_MaxLP maximum speed since last zero speed in RPMInputFLOATSynCk_PermL25A_PERM - sync check permissiveOutputBITOnLineOS1TstL97HP_TST1 - online HP vverspeed testOutputBITOnLineOS1XL43EOST_ONL - online HP overspeed testOutputBITOnLineOS1TstL97HP_TST2 - online IP overspeed testOutputBITOffLineOS1TstL97HP_TST2 - online HP overspeed testOutputBITOffLineOS1TstL97HP_TST2 - online IP overspeed testOutputBITOffLineOS1TstL97HP_TST2 - online IP overspeed testOutputBITOffLineOS1TstL97HP_TST2 - online IP overspeed testOutputBIT<	L5Cont1_Trip	Contact 1 trip	Input	BIT
LPShaftLockLP shaft lockedInputBITBus FreqSFL 2 HzInputFLOATGenFreqSF 2 HzInputFLOATGen VoltsDiffDV_ERR kV rms - generator low is negativeInputFLOATGenFreqDiffSFDIFF2 slip Hz - generator slow is negativeInputFLOATGenPhaseDiffSSDIFF2 phase degrees - generator lag is negativeInputFLOATPR1_AccelHP accelerate in RPM/secondInputFLOATPR2_AccelIP accelerate in RPM/secondInputFLOATPR3_AccelLP accelerate in RPM/secondInputFLOATPR4_MaxHP maximum speed since last zero speed in RPMInputFLOATPR3_MaxLP maximum speed since last zero speed in RPMInputFLOATPR3_MaxLP maximum speed since last zero speed in RPMInputFLOATSynCk_PermL25A_PERM - sync check permissiveOutputBITSynCk_ByPassL25A_PERM - sync check permissiveOutputBITOnLineOS1TstL97HP_TST1 - online HP vverspeed testOutputBITOnLineOS1XL43EOST_ONL - online HP overspeed testOutputBITOnLineOS1TstL97HP_TST1 - online HP overspeed testOutputBITOnLineOS1TstL97HP_TST2 - online HP overspeed testOutputBITOffLineOS1TstL97HP_TST2 - online HP overspeed testOutputBITOffLineOS1TstL97HP_TST2 - online HP overspeed testOutputBITOffLineOS1TstL97HP_TST2 - online HP overspeed test <td< td=""><td>:</td><td>:</td><td>Input</td><td>BIT</td></td<>	:	:	Input	BIT
Bus Freq SFL 2 Hz Input FLOAT GenFreq SF 2 Hz Input FLOAT GenVoltsDiff DV_ERR kV rms - generator low is negative Input FLOAT GenFreqDiff SFDIFF2 slip Hz - generator slow is negative Input FLOAT GenPhaseDiff SSDIFF2 phase degrees - generator lag is negative Input FLOAT PR1_Accel HP accelerate in RPM/second Input FLOAT PR3_Accel LP accelerate in RPM/second Input FLOAT PR1_Max HP maximum speed since last zero speed in RPM Input FLOAT PR2_Max IP maximum speed since last zero speed in RPM Input FLOAT PR3_Max LP maximum speed since last zero speed in RPM Input FLOAT SynCk_Perm L25A_PERM - sync check permissive Output BIT SynCk_ByPass L25A_PERM - sync check papass Output BIT OnLineOS1Tst L97HP_TST1 - online HP overspeed test Output BIT OnLineOS1X L43EOST_ONL - online HP overspeed test Output BIT OnLin	L5Cont7_Trip	Contact 7 trip	Input	BIT
GenFreqSF 2 HzInputFLOATGen VoltsDiffDV_ERR kV rms - generator low is negativeInputFLOATGenFreqDiffSFDIFF2 slip Hz - generator slow is negativeInputFLOATGenPhaseDiffSSDIFF2 phase degrees - generator lag is negativeInputFLOATPR1_AccelHP accelerate in RPM/secondInputFLOATPR2_AccelIP accelerate in RPM/secondInputFLOATPR3_AccelLP accelerate in RPM/secondInputFLOATPR1_MaxHP maximum speed since last zero speed in RPMInputFLOATPR2_MaxIP maximum speed since last zero speed in RPMInputFLOATPR3_MaxLP maximum speed since last zero speed in RPMInputFLOATSynCk_PermL25A_PERM - sync check permissiveOutputBITSynCk_ByPassL25A_BYPASS - sync check bypassOutputBITOnLineOS1TstL97HP_TST1 - online HP overspeed testOutputBITOnLineOS2TstL97IP_TST1 - online IP overspeed testOutputBITOffLineOS1TstL97HP_TST2 - offline IP overspeed testOutputBITOf	LPShaftLock	LP shaft locked	Input	BIT
Gen VoltsDiffDV_ERR kV rms - generator low is negativeInputFLOATGenFreqDiffSFDIFF2 slip Hz - generator slow is negativeInputFLOATGenPhaseDiffSSDIFF2 phase degrees - generator lag is negativeInputFLOATPR1_AccelHP accelerate in RPM/secondInputFLOATPR3_AccelIP accelerate in RPM/secondInputFLOATPR3_AccelLP accelerate in RPM/secondInputFLOATPR1_MaxHP maximum speed since last zero speed in RPMInputFLOATPR3_MaxIP maximum speed since last zero speed in RPMInputFLOATPR3_MaxLP maximum speed since last zero speed in RPMInputFLOATSynCk_PermL25A_PERM - sync check permissiveOutputBITSynCk_ByPassL25A_BYPASS - sync check bypassOutputBITOnLineOS1TstL97HP_TST1 - online HP overspeed testOutputBITOnLineOS2TstL97IP_TST1 - online HP overspeed testOutputBITOffLineOS1TstL97HP_TST2 - online HP overspeed testOutput <td>Bus Freq</td> <td>SFL 2 Hz</td> <td>Input</td> <td>FLOAT</td>	Bus Freq	SFL 2 Hz	Input	FLOAT
GenFreqDiffSFDIFF2 slip Hz - generator slow is negativeInputFLOATGenPhaseDiffSSDIFF2 phase degrees - generator lag is negativeInputFLOATPR1_AccelHP accelerate in RPM/secondInputFLOATPR2_AccelIP accelerate in RPM/secondInputFLOATPR3_AccelLP accelerate in RPM/secondInputFLOATPR1_MaxHP maximum speed since last zero speed in RPMInputFLOATPR2_MaxIP maximum speed since last zero speed in RPMInputFLOATPR3_MaxLP maximum speed since last zero speed in RPMInputFLOATSynCk_PermL25A_PERM - sync check permissiveOutputBITSynCk_ByPassL25A_BYPASS - sync check bypassOutputBITOnLineOS1TstL97HP_TST1 - online HP vverspeed testOutputBITOnLineOS1TstL97IP_TST1 - online IP overspeed testOutputBITOffLineOS1TstL97IP_TST2 - online HP overspeed testOutputBITOffLineOS1TstL97IP_TST2 - online HP overspeed testOutputBITOffLineOS1TstL97IP_TST2 - offline IP overspeed testOutputBITOffLineOS1TstL97IP_TST2 - offline IP overspeed testOutputBITOffLineOS3TstL97IP_TST2 - offline IP overspeed testOutput </td <td>GenFreq</td> <td>SF 2 Hz</td> <td>Input</td> <td>FLOAT</td>	GenFreq	SF 2 Hz	Input	FLOAT
GenPhaseDiffSSDIFF2 phase degrees - generator lag is negativeInputFLOATPR1_AccelHP accelerate in RPM/secondInputFLOATPR2_AccelIP accelerate in RPM/secondInputFLOATPR3_AccelLP accelerate in RPM/secondInputFLOATPR1_MaxHP maximum speed since last zero speed in RPMInputFLOATPR2_MaxIP maximum speed since last zero speed in RPMInputFLOATPR3_MaxLP maximum speed since last zero speed in RPMInputFLOATSynCk_PermL25A_PERM - sync check permissiveOutputBITSynCk_ByPassL25A_BYPASS - sync check bypassOutputBITOnLineOS1TstL97HP_TST1 - online HP vverspeed testOutputBITOnLineOS1TstL97IP_TST1 - online IP overspeed testOutputBITOnLineOS1TstL97HP_TST2 - online HP overspeed testOutputBITOffLineOS1TstL97HP_TST2 - offline IP overspeed testOutputBI	Gen VoltsDiff	DV_ERR kV rms - generator low is negative	Input	FLOAT
PR1_AccelHP accelerate in RPM/secondInputFLOATPR2_AccelIP accelerate in RPM/secondInputFLOATPR3_AccelLP accelerate in RPM/secondInputFLOATPR1_MaxHP maximum speed since last zero speed in RPMInputFLOATPR2_MaxIP maximum speed since last zero speed in RPMInputFLOATPR3_MaxLP maximum speed since last zero speed in RPMInputFLOATSynCk_PermL25A_PERM - sync check permissiveOutputBITSynCk_ByPassL25A_BYPASS - sync check bypassOutputBITOnLineOS1TstL97HP_TST1 - online HP vverspeed testOutputBITOnLineOS1XL43EOST_ONL - online HP overspeed testOutputBITOnLineOS1TstL97HP_TST1 - online IP overspeed testOutputBITOnLineOS1TstL97HP_TST2 - online HP overspeed testOutputBITOffLineOS1TstL97HP_TST2 - online HP overspeed testOutputBIT <td< td=""><td>GenFreqDiff</td><td>SFDIFF2 slip Hz - generator slow is negative</td><td>Input</td><td>FLOAT</td></td<>	GenFreqDiff	SFDIFF2 slip Hz - generator slow is negative	Input	FLOAT
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TrpAntcptTst L97A_TST - trip anticipate test Output BIT	OffLineOS2Tst	L97IP_TST2 - offline IP overspeed test	Output	BIT
	OffLineOS3Tst	L97LP_TST2 - offline LP overspeed test	Output	BIT
LokdRotorByp L97LR_BYP - locked rotor bypass Output BIT	TrpAntcptTst	L97A_TST - trip anticipate test	Output	BIT
	LokdRotorByp	L97LR_BYP - locked rotor bypass	Output	BIT

HPZeroSpdByp	L97ZSC_BYP - HP zero speed check bypass	Output	BIT
TestETR1	L97ETR1 - ETR1 test, true deenergizes relay	Output	BIT
:	:	Output	BIT
TestETR4	L97ETR4 - ETR4 test, true deenergizes relay	Output	BIT
PTR1	L20PTR1 - primary trip relay CMD for diagnostic only	Output	BIT
:	:	Output	BIT
PTR6	L20PTR6 - primary trip relay CMD for diagnostic only	Output	BIT
PR_Max_Rst	Maximum speed reset	Output	BIT
CJBackup	Estimated TC CJ temperature in degrees F	Output	FLOAT
OS1_Setpoint	HP overspeed setpoint in RPM	Output	FLOAT
OS2_Setpoint	IP overspeed setpoint in RPM	Output	FLOAT
OS3_Setpoint	LP overspeed detpoint in RPM	Output	FLOAT
OS1_TATrpSp	PR1 overspeed trip setpoint in RPM for trip anticipate Fn	Output	FLOAT
CPD	Compressor discharge pressure for overtemperature trip CPD bias	Output	FLOAT
DriveFreq	Drive (generator) frequency (Hz), used for non standard drive configuration	Output	FLOAT

I/O Board Alarms

Diagnostic alarms for any I/O board can be displayed and reset from the toolbox. For troubleshooting and general diagnostic alarm information refer to GEG-6421 Volume I, Chapter 8.

I/O Board Diagnostic Alarms

Board	Fault	Fault Description	Possible Cause
VPRO	2	Flash Memory CRC Failure	Board firmware programming error (board will not go online)
	3	CRC failure override is active	Board firmware programming error (board is allowed to go online)
	16	System Limit Checking is Disabled	System checking was disabled by configuration.
	17	Board ID Failure	Failed ID chip on the VME I/O board
	18	J3 ID Failure	Failed ID chip on connector J3, or cable problem
	19	J4 ID Failure	Failed ID chip on connector J4, or cable problem
	20	J5 ID Failure	Failed ID chip on connector J5, or cable problem
	21	J6 ID Failure	Failed ID chip on connector J6, or cable problem
	22	J3A ID Failure	Failed ID chip on connector J3A, or cable problem
	23	J4A ID Failure	Failed ID chip on connector J4A, or cable problem
	24	Firmware/Hardware Incompatibility	Invalid terminal board connected to VME I/O board
	30	ConfigCompatCode mismatch; Firmware: #; Tre: # The configuration compatibility code that the firmware is expecting is different than what is in the tre file for this board	A tre file has been installed that is incompatible with the firmware on the I/O board. Either the tre file or firmware must change. Contact the factory.
	31	IOCompatCode mismatch; Firmware: #; Tre: # The I/O compatibility code that the firmware is expecting is different than what is in the tre file for this board	A tre file has been installed that is incompatible with the firmware on the I/O board. Either the tre file or firmware must change. Contact the factory.
	32-38	Contact Input # Not Responding to Test Mode. Trip interlock number # is not reliable	Contact input circuit failure on VPRO or TREG board.
	39-40	Contact Excitation Voltage Test Failure. Contact excitation voltage has failed, trip interlock monitoring voltage is lost	Loss of P125 voltage caused by disconnection of JH1 to TREG, or disconnect of JX1, JY1, JZ1 on TREG to J3 on VPRO.

41-43	Thermocouple ## Raw Counts High. The ## thermocouple input to the analog to digital converter exceeded the converter limits and will be removed from scan	A condition such as stray voltage or noise caused the input to exceed +63 millivolts.
44-46	Thermocouple ## Raw Counts Low. The ## thermocouple input to the analog to digital converter exceeded the converter limits and will be removed from scan	The board detected a thermocouple open and applied a bias to the circuit driving it to a large negative number, or the TC is not connected, or a condition such as stray voltage or noise caused the input to exceed –63 millivolts.
47	Cold Junction Raw Counts High. Cold junction device input to the A/D converter has exceeded the limits of the converter. Normally two cold junction inputs are averaged; if one is detected as bad then the other is used. If both cold junctions fail, a predetermined value is used	The cold junction device on the terminal board has failed.
48	Cold Junction Raw Counts Low. Cold junction device input to the A/D converter has exceeded the limits of the converter	The cold junction device on the terminal board has failed.
49	Calibration Reference # Raw Counts High. Calibration reference # input to the A/D converter exceeded the converter limits. If Cal. Ref. 1, all even numbered TC inputs will be wrong; if Cal. Ref. 2, all odd numbered TC inputs will be wrong	The precision reference voltage on the board has failed.
50	Calibration Reference Raw Counts Low. Calibration reference input to the A/D converter exceeded the converter limits	The precision reference voltage on the board has failed.
51	Null Reference Raw Counts High. The null (zero) reference input to the A/D converter has exceeded the converter limits	The null reference voltage signal on the board has failed.
52	Null Reference Raw Counts Low. The null (zero) reference input to the A/D converter has exceeded the converter limits	The null reference voltage signal on the board has failed.
53-55	Thermocouple ## Linearization Table High. The thermo- couple input has exceeded the range of the linearization (lookup) table for this type. The temperature will be set to the table's maximum value	The thermocouple has been configured as the wrong type, or a stray voltage has biased the TC outside of its normal range, or the cold junction compensation is wrong.
56-58	Thermocouple ## Linearization Table Low. The thermo - couple input has exceeded the range of the linearization (lookup) table for this type. The temperature will be set to the table's minimum value	The thermocouple has been configured as the wrong type, or a stray voltage has biased the TC outside of its normal range, or the cold junction compensation is wrong.
59-61	Analog Input # Unhealthy. The number # analog input to the A/D converter has exceeded the converter limits	The input has exceeded $4-20 \text{ mA}$ range, or for input #1 if jumpered for $\pm 10 \text{ V}$, it has exceeded $\pm 10 \text{ V}$ range, or the 250 ohm burden resistor on TPRO has failed.
63	P15=####.## Volts is Outside of Limits. The P15 power supply is out of the specified +12.75 to +17.25 V operating limits	Analog ± 15 V power supply on VPRO board has failed.

64	N15=####.## Volts is Outside of Limits. The N15 power supply is out of the specified –17.25 to –12.75 V operating limits	Analog ± 15 V power supply on VPRO board has failed.
67	P28A=####.## Volts is Outside of Limits. The P28A power supply is out of the specified 23.8 to 31.0 V operating limits	The P28A power supply on VPWR board has failed, test P28A at VPRO front panel, otherwise there may be a bad connection at J9, the VPWR to VPRO interconnect.
68	P28B=####.## Volts is Outside of Limits. The P28B power supply is out of the specified 23.8 to 31.0 V operating limits	The P28B power supply on VPWR board has failed, test P28B at VPRO front panel, otherwise there may be a bad connection at J9, the VPWR to VPRO interconnect.
69-71	Trip Relay (ETR) Driver # Mismatch Requested State.	The ETR # relay driver or relay driver
77-79	The state of the command to the Emergency Trip Relay (ETR) does not match the state of the relay driver feedback signal; the ETR cannot be reliably driven until corrected	feedback monitor on the TREG terminal board has failed, or the cabling between VPRO and TREG is incorrect.
75	Servo Clamp Relay Driver Mismatch Requested State. The state of the command to the servo clamp relay does not match the state of the servo clamp relay driver feedback signal; cannot reliably drive the servo clamp relay until corrected	The servo clamp relay driver or relay driver feedback monitor on the TREG board has failed, or the cabling between VPRO and TREG is incorrect.
76	K25A Relay (Synch Check) Driver Mismatch Requested State. The state of the command to the K25A relay does not match the state of the K25A relay driver feedback signal; cannot reliably drive the K25A relay until corrected	K25A relay driver or relay driver feedback on the TREG board has failed, or the cabling between VPRO and TREG is incorrect.
83-85 91-93	Trip Relay (ETR) Contact # Mismatch Requested State. The state of the command to the ETR does not match the state of the ETR contact feedback signal; the ETR cannot be reliably driven until corrected	The relay driver on TREG may have failed, or the ETR on the TREG board has failed, or the cabling between the VPRO and TREG is incorrect.
99-104	TREG Solenoid Voltage # Mismatch Requested State. The state of the trip solenoid # does not match the command logic of the voted ETR # on TREG, and the voted primary trip relay (PTR) # on TRPG, the ETR cannot be reliably driven until corrected	The trip solenoid # voltage monitor on TREG has failed or ETR # driver failed, or PTR # driver failed. There may be a loss of 125 V dc via the J2 connector from TRPG, which has a diagnostic.
72-74	Econ Relay Driver # Mismatch Requested State. The	Economizing relay driver # or relay
80-82	state of the command to the economizing relay does not match the state of the economizing relay driver feedback signal; cannot reliably drive the economizing relay until corrected	driver feedback monitor on TREG board has failed, or the cabling between VPRO and TREG is incorrect.
86-88	Econ Relay Contact # Mismatch Requested State. The	Economizing relay driver # on TREG
94-96	state of the command to the economizing relay does not match the state of the economizing relay contact feedback signal; cannot reliably drive the economizing relay until corrected	board has failed, or the economizing relay on TREG has failed, or the cabling between VPRO and TREG is incorrect.
90	K25A Relay (Synch Check) Coil Trouble, Cabling to P28V on TTUR. The state of the command to the K25A relay does not match the state of the K25A relay contact feedback signal; cannot reliably drive the K25A relay until the problem is corrected. The signal path is from VPRO to TREG to TRPG to VTUR to TTUR	The K25A relay driver or relay driver feedback on the TREG board has failed, or the K25A relay on TTUR has failed, or the cabling between VPRO and TTUR is incorrect.

89	Servo Clamp Relay Contact Mismatch Requested State. The state of the command to the servo clamp relay does not match the state of the servo clamp relay contact feedback signal; cannot reliably drive the servo clamp relay until corrected	The servo clamp relay driver or the servo clamp relay on the TREG board has failed, or the cabling between VPRO and TREG is incorrect.
97	TREG J3 Solenoid Power Source is Missing. The P125 V dc source for driving the trip solenoids is not detected; cannot reliably drive the trip solenoids	The power detection monitor on the TREG1 board has failed, or there is a loss of P125 V dc via the J2 connector from TRPG board, or the cabling between VPRO and TREG1 or between TREG1 and TRPG is incorrect.
98	TREG J4 Solenoid Power Source is Missing. The P125 V dc source for driving the trip solenoids is not detected; cannot reliably drive the trip solenoids K4-K6	The power detection monitor on the TREG2 board has failed, or there is a loss of P125 V dc via the J2 connector from TRPG board, or the cabling between VPRO and TREG2 or between TREG2 and TRPG is incorrect. Also trip relays K4-K6 may be configured when there is no TREG2 board.
105	TREL/S, J3, Solenoid Power, Bus A, Absent. The voltage source for driving the solenoids is not detected on Bus A; cannot reliably drive these solenoids	Loss of power bus A through J2 connector from TRPL/S
106	TREL/S, J3, Solenoid Power, Bus B, Absent. The voltage source for driving the solenoids is not detected on Bus B; cannot reliably drive these solenoids	Loss of power bus B through J2 connector from TRPL/S
107	TREL/S, J3, Solenoid Power, Bus C, Absent. The voltage source for driving the solenoids is not detected on Bus C; cannot reliably drive these solenoids	Loss of Power Bus C through J2 connector from TRPL/S
128-319	Logic Signal # Voting mismatch. The identified signal from this board disagrees with the voted value	A problem with the input. This could be the device, the wire to the terminal board, the terminal board, or the cable.
320-339	Input Signal # Voting mismatch, Local #, Voted #. The specified input signal varies from the voted value of the signal by more than the TMR Diff Limit	A problem with the input. This could be the device, the wire to the terminal board, the terminal board, or the cable.



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VME Power Supply

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Safety Symbol Legend



Indicates a procedure or condition that, if not strictly observed, could result in damage to or destruction of equipment or data.

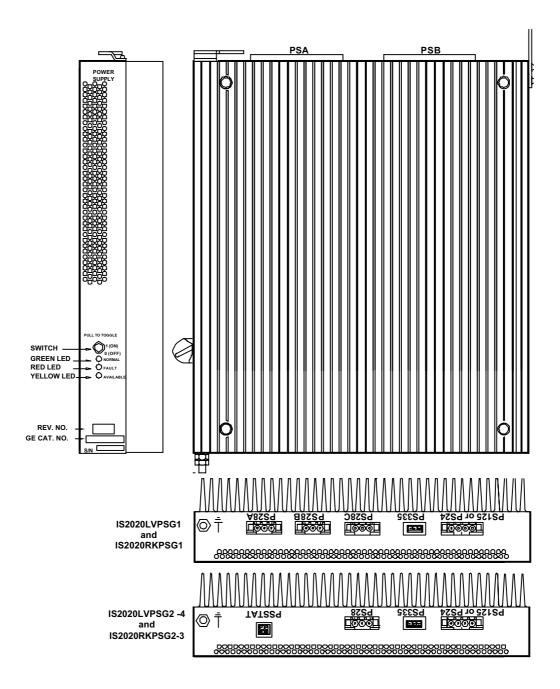
Indicates a procedure, practice, condition, or statement that, if not strictly observed, could result in personal injury or death.

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Diagnostics and Troubleshooting	
Removal and Installation	

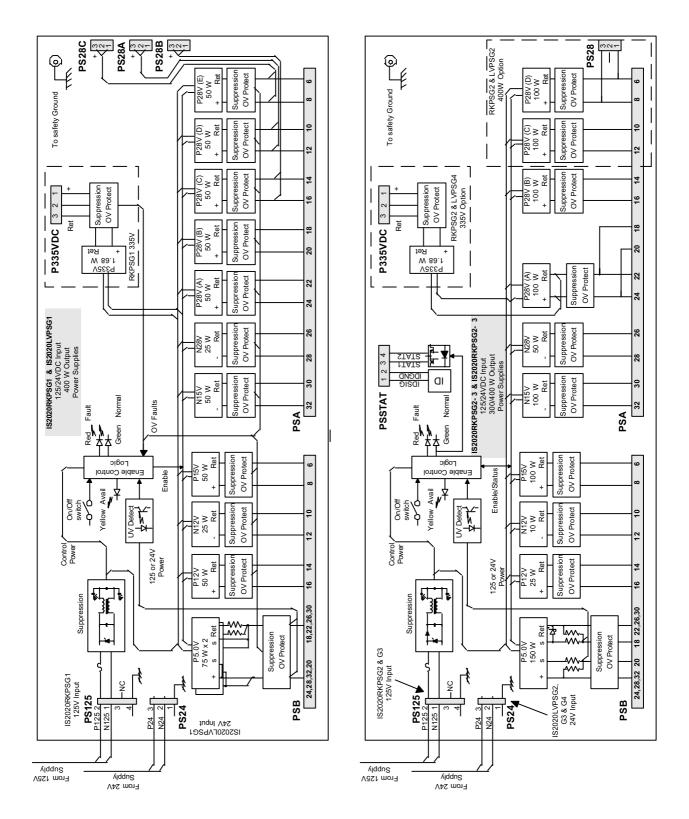
VME Rack Power Supply

The VME rack power supply mounts on the side of the VME control and interface modules. It supplies $+5, \pm 12, \pm 15$, and ± 28 V dc to the VME backplane and an optional 335 V dc output is provided for powering flame detectors connected to TRPG. Two supply input voltage selections are available. There is a 125 V dc input supply that is powered from a Power Distribution Module (PDM) and a low voltage version for 24 V dc operation.

Note A different power supply is used on the stand-alone control rack which only powers the Mark VI controller, VDSK, and VCMI.



VME Rack Power Supply, Front, Side, and Bottom Views



Block Diagram of RKPS and LVPS VME of the Power Supplies

There are currently seven major variations of the VME rack power supply. These variations provide different power supply input and output requirements. The following table defines these variations.

IS2020 Part Number	Input Voltage	Output Rating	+28V PSA Outputs	+28V Remote Outputs	PS335 Output	Status ID Output	Support Redundant Operation
LVPSG1	24VDC	400W	Qty. 5	Qty. 3	No	No	No
RKPSG1	125VDC	400W	Qty. 5	Qty. 3	Yes	No	No
RKPSG2*	125VDC	400W	Qty. 5	Qty. 1	Yes	Yes	Yes
RKPSG3*	125VDC	400W	Qty. 5	Qty. 1	No	Yes	Yes
LVPSG2*	24VDC	400W	Qty. 5	Qty. 1	No	Yes	Yes
LVPSG3*	24VDC	300W	Qty. 3	None	No	Yes	Yes
LVPSG4*	24VDC	300W	Qty. 3	None	Yes	Yes	Yes

VME Rack Power Supply Option Definitions

*Newer design power supplies

With the exception of the number of remote 28 V outputs, the RKPSG2 and LVPSG2 are designed to be direct replacements for the RKPSG1 and LVPSG1 respectively. These two supplies have been replaced with the newer designs (marked with asterisk in the table above).

Operation

The VMERack power supply has only one user control, the power switch, and three status LED indicators. The power switch provides front control of the power supply output voltages and when toggled serves as a fault reset. The yellow, red and green LEDs indicate the status of the input power, fault presence and normal operation.

Power Switch:

The front panel power switch is a locking type that must be pulled out to change position. This switch is a low voltage control to enable or disable the output voltages. If the red LED is ON indicating a fault condition the power switch can be toggled OFF and then back ON again to clear the fault. The fault will only be cleared if the condition the caused it no longer exists.

Yellow LED:

When the power switch is OFF the yellow LED will indicate the status of the input power. If this LED is ON there is power present on the supply input connector. For the newer design, the yellow LED will only turn ON if the input voltage is above the input under voltage fault threshold.

Red LED

This LED will only be ON if there is input power, the power switch is ON and a fault has been detected.

Green LED/Status Output:

If there is input power, the power switch is ON, and there are no detectable faults, the Green LED will be ON. The newer designs also have a status output that mimics the status of this LED. The status output is a NO solid state relay contact that will be CLOSED when the green LED is ON.

Newer supply designs also have a status output that mimics the status of the green LED and an ID output that uniquely identifies the supply back to the system.

Fault Conditions

There are three classes of faults:

- Those that transiently shutdown an output
- Those that require some reset action to clear
- Permanent failures that require the replacement of the supply.

This section describes the first two fault classes and assumes the cause of the fault is external. For a detailed fault diagnostics, refer to the section, *Diagnostics and Troubleshooting*.

If an overcurrent condition exists on an output, the voltage on that output will fold back as required to maintain the constant current limit output. For every output other than the 5 V supply, this condition is not detectable at the supply and the green LED will remain ON. Detection of a low output voltage due to excessive output current has to be detected at the system level through the power supply voltage monitoring. The newer design also has an over temperature monitor of the output modules and a current limit detector on the optional 335V supply. These additional fault detectors may cause the red LED to come on when an output is in current limit but the red LED will also go out when the output voltage returns to normal.

The 5 V current limit is a special case due to the 5 V undervoltage detector. If the current limit causes the 5 V output voltage to fold back below the UV threshold, all of the other outputs will be disabled until the 5 V output voltage returns to a voltage above the UV threshold.

All of the other faults will shut down one or all of the outputs until the external cause of the fault condition is removed and the supply is reset. A reset can be initiated through the front panel power switch or by removing and reapplying input power to the supply. Output overvoltage faults on the newer design require the removal of input power for a minimum of one minute to reset the fault once the source of the fault has been removed. Below is a power supply fault summary.

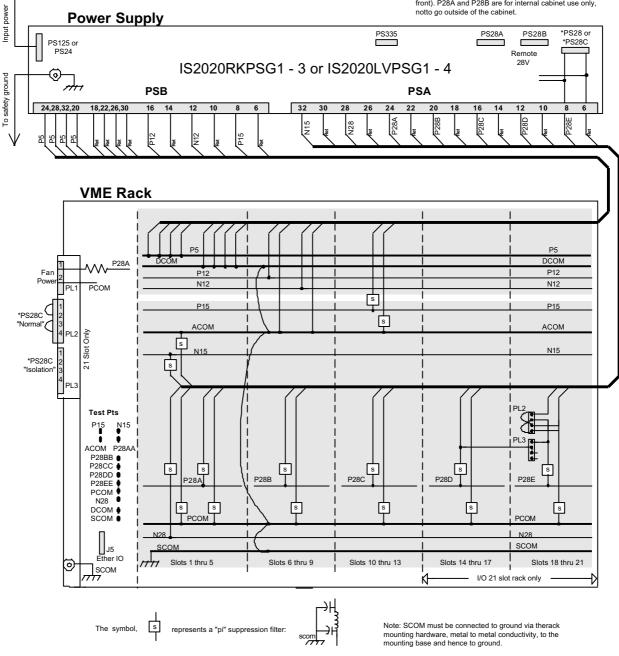
- Input undervoltage (Latched)
- Input overvoltage (Newer Design Only)
- P5 output undervoltage
- Output overvoltage (Latched)
- Over temperature (Newer Design Only)

The following figure shows the power supply connections to the VME rack and the distribution of the power supply outputs.

When the external condition causing the current limit condition is corrected, the output voltage will return to normal.

* PS28 or PS28C Configuration:

Note: The power supply PS28 or PS28C may be isolated from the I/O rack for external use. One plug, two positions Normal (PL2), Isolation (PS3), for selection; Plug is located on left side of rack (from the front). P28A and P28B are for internal cabinet use only, notto go outside of the cabinet.



VME I/O Rack Power Supply and Cables

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Diagnostics

Incoming and outgoing voltages and currents are monitored for control and protection purposes. If the red LED is ON, this is not a direct indication that the power supply has failed and has to be replaced. The LED ON could indicate that something is wrong in the system and the fault LED is latched on. The following is a description of the power supply parameters that are monitored and the conditions that can cause faults.

Input Undervoltage (below the minimum operating voltage)

The input voltage has to be above the undervoltage threshold or operation of the supply will be inhibited. For the newer design this is indicated by no LEDs ON. The red LED will come ON and remain on until the input voltage is above the undervoltage threshold and the power switch is toggled. If an undervoltage fault occurs during normal operation, the outputs will be disabled and the red LED will come ON and remain ON until the input voltage is above the undervoltage threshold and the power switch is toggled.

Input Overvoltage (newer design above maximum operating voltage)

If the supply power switch is turned on in this condition there, will be no output voltages and the red LED will come ON and remain on until the input voltage is below the overvoltage threshold and the power switch is toggled. If an overvoltage fault occurs during normal operation, the outputs will be disabled and the red LED will come ON and remain ON until the input voltage is below the over voltage threshold and the power switch is toggled.

5 V Output Undervoltage (typically below 4.7 V)

The P5 output voltage has to be above the undervoltage threshold or operation of the supply will be inhibited, all supply outputs will be turned off, and the red LED will be ON. If an undervoltage fault occurs during normal operation, the outputs will be disabled and the red LED will come ON and remain ON until the output voltage is above the undervoltage threshold.

5 V Output Overvoltage (typically above 6 V)

The P5 output voltage has to be below the overvoltage threshold or operation of the supply will be inhibited. All supply outputs will be latched OFF and the red LED will be ON until the power switch is toggled. For the newer design, this fault must be reset by removing input power to the supply (wait for one minute and re-apply input power).

Output Overvoltage other than P5 (typically above 120%)

The output voltage has to be below the overvoltage threshold or operation of the supply output that is above the threshold will be inhibited (latched OFF) until the power switch is toggled. The red LED will be ON during this fault. For the newer design, this fault must be reset by removing input power to the supply (wait for one minute and re-apply input power).

Output Overtemperature (newer design typically above 100 degrees C)

The modules that supply the output voltage have to be operated below the overtemperature threshold. A specific supply output module operated above the threshold will be inhibited until the temperature is lowered below the threshold. The red LED will be ON during this fault. An overtemperature of the 5 V module will cause a 5 V undervoltage fault.

If the supply power switch is turned on in this condition there will be no output voltages.

The input voltage has to be below the overvoltage threshold or operation of the supply will be inhibited and the yellow LED will be ON.

Troubleshooting

The supply has no field serviceable components. If a supply is found to be defective it must be replaced. The power supply cover should not be removed in the field.

There are only two indications of a problem on the power supply itself. A problem is indicated when there are no LEDs ON or the red LED is ON. Both conditions will be annunciated on the newer designs through the status output.

No LEDs ON is a good indication of an input voltage problem or a defective supply. If the red LED is ON, the cause could be any of the fault conditions listed above or a defective supply. Below is a list of troubleshooting hints.

Note Overvoltage faults on the newer design must be reset by removing input power to the supply, waiting for one minute, and re-applying input power.

No LEDs ON

Verify that the input connector and voltage to the supply are correct. If they are, then replace the supply. Use caution when powering on the replacement supply because the failure could have been caused by a problem in the system.

Red LED ON and system up

This condition indicates that the 5 V power is OK. Use the system diagnostics and or testpoints on the left bottom of the control rack or at the supply connectors to find the faulted outputs. Try and clear the fault with the input power or switch reset. If the green LED comes ON, the fault was a transient one and may come back. If the red LED is still ON, remove the connector supplying the faulted output and reset the supply. If the red LED is still ON, then a defective supply is the most probable cause. If the green LED comes ON, then the problem is most likely in the system.

Red LED ON and system down

This condition indicates that the 5 V power is not OK. In this case, all of the supply outputs should be off. Try and reset the fault with the input power. If the green LED comes on the fault was a transient one and may come back. If the red LED is still ON, remove the PSA/PSB output connector at the top of the supply and reset the supply. If the red LED is still ON, then a defective supply is the most probable cause. If the green LED comes ON, then the problem is most likely in the system.

Green LED ON and system up but one or more of the voltages out of specification

This condition indicates that the 5 V power is OK. Each supply output has a current limit and short circuit protection. This condition could be caused by a short or failed component in the system. Remove the connector supplying the failed output voltage. If the voltage returns to normal this is an indication of a system problem. If the voltage does not return to normal then the most probable cause is a defective supply.

Thermal overtemperature faults (new design only)

Even in the worst case ambient conditions, a thermal fault should not occur if the outputs are not overloaded. A sustained current limit on a supply output will be the most likely cause of a thermal fault.

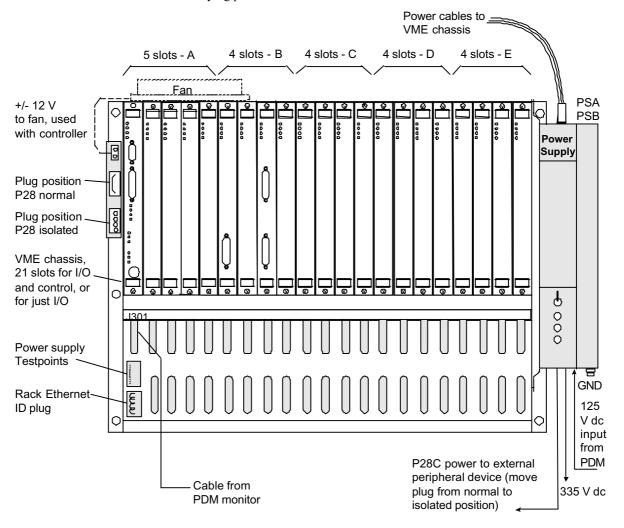
Specifications Power Supply Specifications

Item		Descrip	tion				
Input v	oltage						
	125 V	70 V to 145 V dc floating supply Up to 10 V pp ripple					
input		18.5 V to 32 V dc floating supply Up to 2 V pp ripple					
	24 V input						
Input underv	oltage		Undervoltage protection provided to prevent supply operation when the input voltage below the minimum operating level.				
Input o	vervoltage*		age protection protection protection protection		event supply op	peration when	the input voltage is
Isolatio	n	True iso	lation from input to	o output, 15	500 V		
Output	voltages	Output Voltage	Voltage	Voltage R	egulation	Capacity	Typical Over
For the and LV supplie		P5 P15 N15 P12 N12	+5 V dc +15 V dc -15 V dc +12 V dc -12 V dc	Less than Less than Less than Less than Less than	± 3% ± 3% ± 3%	150 Watts 50 Watts 50 Watts 50 Watts 25 Watts	$\begin{array}{c} 120\%\pm5\%\\ 120\%\pm5\%\\ 120\%\pm5\%\\ 120\%\pm5\%\\ 120\%\pm5\%\\ 120\%\pm5\%\\ 120\%\pm5\%\end{array}$
		P28 N28 P335	+28 V dc -28 V dc +335 V dc	Less than Less than Less than Less than	± 5% ± 5%	50 Watts 50 Watts 25 Watts 1.68 Watts	$120\% \pm 5\%$ $120\% \pm 5\%$ $120\% \pm 5\%$ 110% to $120%$
	RKPSG2 - VPSG2 - 4 s*	P5 P15 N15	+5 V dc +15.35 V dc -15.35 V dc	Less than Less than Less than	± 3% ± 3%	150 Watts 100 Watts 100 Watts	$\begin{array}{c} 130\% \pm 5\% \\ 120\% \pm 5\% \\ 120\% \pm 5\% \end{array}$
supplie	voltage	P12 N12 P28 N28 P335	+12.3 V dc -12.3 V dc +28 V dc -28 V dc +335 V dc	Less than Less than Less than Less than Less than	± 3% ± 5% ± 5%	25 Watts 10 Watts 100 Watts 50 Watts 1.68 Watts	$120\% \pm 5\%$ $120\% \pm 5\%$ $120\% \pm 5\%$ $120\% \pm 5\%$ $120\% \pm 5\%$ 110% to $120%$
Power sequer	cing	The 5 V dc supply comes up first, then all the others					
Total O	utput	Maximu	m of 400 Watts				
Total o LVPSG	utput 3 & 4 only*	Maximum of 300 Watts					
Short c	ircuit	Short circuit protection on all power supplies, with self-recovery. Note: A 5 V short circuit on the new design will cause a latched fault.					
Tempe	rature	Ambient air convection cooling 0 to 60 degree C					
Indicat	ing lights	Green: Red:	Normal Fault	Status is (Power is a		or more outpu	uts off due to a fault.
			Available		•••		
Chat		Yellow: Available Power is applied, but switch is OFF NO SSR contact .5A @ 55V dc - Closed when the green indicating light is on					
	output*		_		-	-	
ID tag o	output*	Dallas D revision	S2502 output. 25	502 data = \	Neek & year tes	sted, unit num	ber, part number and

*Only pertain to the newer design power supplies

Removal and Installation

The power supply is mounted to the right-hand side of the VME rack on a sheet metal bracket. The dc input, 28 V dc output, and 335 V dc output connections are at the bottom. The newer design also has a status connector on the bottom. Two connectors, PSA and PSB, at the top of the assembly mate with a cable harness carrying power to the VME rack.



Power Supply, VME Chassis, and Cabling to External Devices

Each of the five 28 V dc power modules supplies a section of the VME rack. These sections are labeled A, B, C, D, E, and F. The P28C output or PS28 at the bottom of the power supply can be used to power an external peripheral device. To do this the jumper plug shown on the bracket to the left of the rack must be moved from the *Normal* position to the *Isolated* position below.

The fan is only used when the controller is mounted in the rack. It is powered from the top connector on the same bracket, located on the left side of the rack.



To prevent electric shock, turn off power to the RPSM to be replaced, then test to verify that no power exists on the module before touching it or any connected circuits.

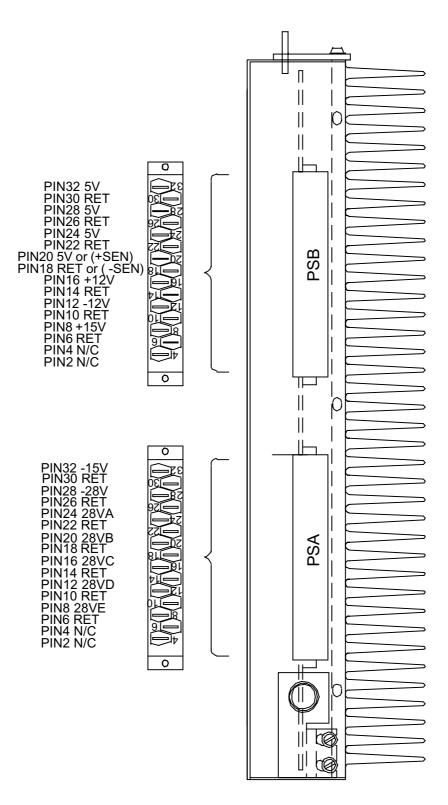


To prevent equipment damage, do not remove, insert, or adjust any connections while power is applied to the equipment.

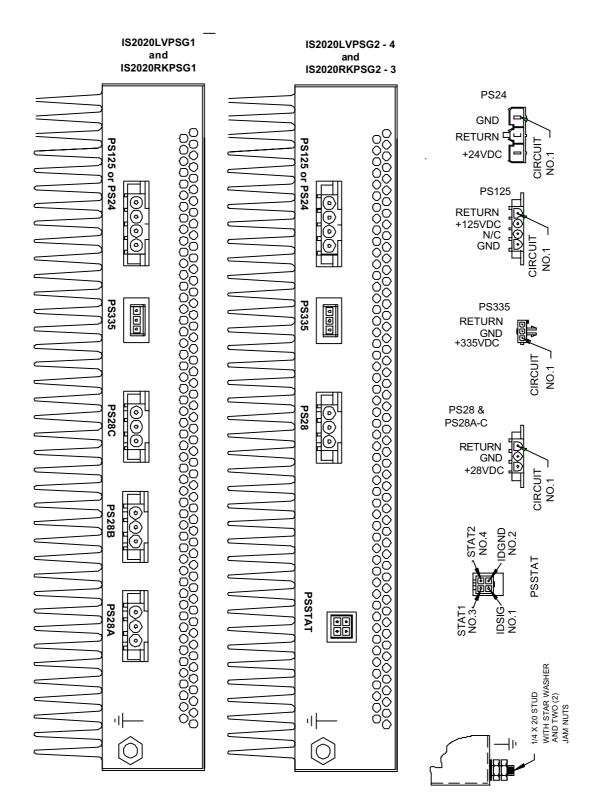
- > To remove the power supply (see figures below)
- 1. Loosen the PSA/PSB bracket captive fastener at the top front of the supply.
- 2. Separate the PSA/PSB bracket assembly from the supply.
- 3. Disconnect the bottom connectors.
- 4. Loosen the two sheet metal bracket captive fasteners.
- 5. Pull the sheet metal bracket/power supply assembly forward and off of the control rack.
- 6. Remove the four mounting bolts that hold the power supply to the bracket and remove the supply.

Note Reinstall the bolts and bracket on the control rack if a replacement supply is not going to be installed.

- > To install the power supply (see figures below)
- 1. Locate the supply mounting sheet metal bracket and four mounting bolts.
- 2. Position the supply on the bracket heatsink up with the front of the supply at the captive fasteners and install the four mounting bolts from the heatsink side.
- 3. Slide the power supply bracket assembly on to the control rack and tighten the two captive fasteners.
- 4. Slide the PSA/PSB assembly rear tab into the slot on the bracket located athe top rear of the power supply.
- 5. Push the connector assemble into the mating connectors on the top of the supply.
- 6. Tighten the PSA/PSB bracket captive fastener at the top front of the supply.
- 7. Connect the power supply bottom connectors.



Power Supply, Top Connectors

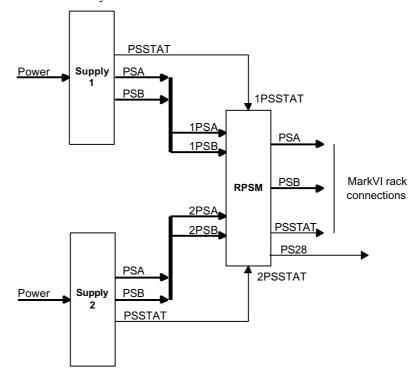


Power Supply, Bottom Connectors

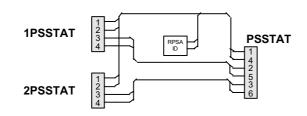
VME Rack Redundant Power Supply Module (RPSM)

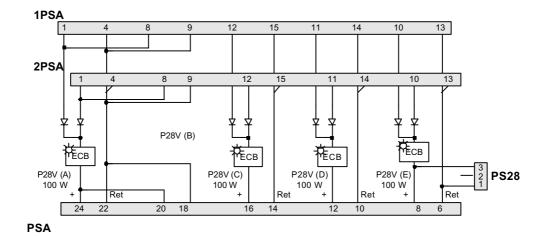
To improve system reliability, the redundant power supply module (RPSM) module can parallel ten output voltages from two independent power supplies. *OR* ing diodes are used to *OR* the outputs of one supply with the outputs from a second redundant supply. Nine of the paralleling circuits have an additional current limit function. All of the output circuits have an LED status indicator.

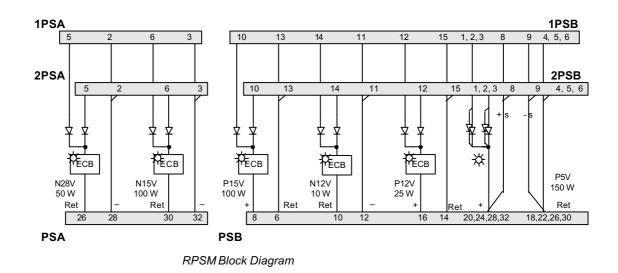
Refer to the table for suitable power supplies for use with RPSM. The following figure shows the power and signal flow for two paralleled power supplies providing power for a Mark VI control rack. To provide redundancy, the outputs of each supply are passed into the RPSM, *OR*ed and the redundant voltages are passed out the RPSM outputs. The RPSM module mounts on the side of the control rack in place of the power supply. The two power supplies that feed the RPSM are remotely mounted.



Power Supply and RPSM Signal Flow







Operation

Output Voltage ORing

The ten outputs of two supplies are *OR*ed together using low forward drop Schottky diodes. If an output of one of the supplies fails, the corresponding output on the other supply will pick up the full load through the diode. It is not intended that the two supplies equally share the load current, but if a short occurs on a RPSM output, it is possible to supply twice the normal short circuit current to the load. To prevent this, all of the outputs of the *OR*ing diodes, with the exception of the 5 V, have an additional current limit circuit.

Refer to the table for expected RPSM output voltages accounting for the voltage losses introduced by passing the supply outputs through the *OR*ing circuits. Due to the wiring impedance between the supply outputs and the RPSM, the supplies will tend to share the load. The sharing will reduce the diode and conductor losses so the expected losses for normal operations will be less than with one supply faulted.

RPSM Voltage Outputs

Output Voltage	Conditions	Min.	Typical	Max.	Units
+5 V	20 – 30 A	4.90	5.05	5.20	V dc
±12 V	0.1 – 1.6 A	11.64	12.0	12.72	V dc
±15 V	0.1 – 5.3 A	14.55	15.0	15.97	V dc
±28 V	0.2 – 3.2 A	26.6	28.0	29.4	V dc

Current Limit ECB

No current limiting is provided on the RPSM module for the 5 V output.

These circuits will hold the

short circuit current to an

acceptable level.

Nine of the outputs have electronic circuit breakers (ECBs) to limit the short circuit current. These circuit breakers are of the auto-reset type. Once the supplied output current exceeds the overcurrent threshold the output will be turned OFF and the reset timer started. Once the reset timer has expired the output will be turned back ON. If the overcurrent condition still exists, the output will be turned OFF and the reset timer started again. This cycle will continue until the short is removed. The output will then return to normal operation.

RPSM Electronic Circuit Breaker Limits

Parameter	Min.	Typical	Max.	Units
Reset Time		500		msec
$\pm 12 \text{ OC Threshold}$	2.78	3.3	3.89	Amps
± 15 OC Threshold	8.30	10	11.70	Amps
± 28 OC Threshold	4.15	5	5.85	Amps

Indicator LEDs

A flashing LED indicates that the output ECB is tripped.

All of the RPSM supply outputs have green status LEDs to indicate that power is being supplied to the load. The LEDs are located on the front panel of the module. For normal operations these LEDs will be ON solid. If the RPSM is not supplying the correct power to the load, one or more of these LEDs are OFF or flashing.

LED Definitions

LED	Description
P5	P5 output voltage indicator
P12	P12 output voltage indicator
N12	N12 output voltage indicator
P15	P15 output voltage indicator
N15	N15 output voltage indicator
N28	N28 output voltage indicator
P28AB	P28A/B output voltage indicator
P28C	P28C output voltage indicator
P28D	P28D output voltage indicator
P28E	P28E output voltage indicator

Parallel Status/ID

Each status connector from the power supplies has a status and ID signal. The ID signals from the two supplies are wired together along with the ID signal from the RPSM and passed out through the PSSTAT connector. The ID signal output is a single wire LAN line with three DALLAS 2502 ID ICs connected on it. The NO SSR contact status signals from the both supplies are passed through the RPSM and out the PSSTAT connector.

Power Supply 1 and 2 Status SSR NO Contacts

Parameter	Conditions	Min.	Typical	Max.	Units
V dc rating		55			V dc
V ac rating		55			V peak
Current rating		500			mA
ON resistance				1.0	Ohm
Isolation	Input to output	1500			V dc

Diagnostics and Troubleshooting

There are no field serviceable components in the RPSM module. If one or more of the green front panel LEDs are OFF, this is not a direct indication that the RPSM module has failed and has to be replaced. An LED OFF could indicate that something is wrong in the system and the fault is not due to the RPSM module. Below is a list of fault indications and the possible causes.

All **RPSM green LEDs OFF** - This is an indication of a problem back at the power supplies and not an RPSM failure.

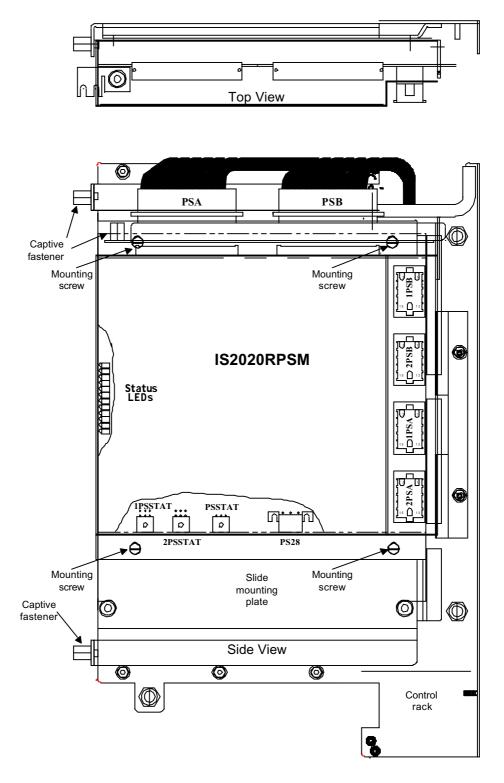
One or more RPSMgreen LEDs OFF (but not all) - An RPSM LED OFF condition is an indication that there is no output voltage due to a short in the control rack or an RPSM failure.

5 V output problems - The 5 V output is unique from all of the other outputs. This RPSM output does not have current limit protection and has remote voltage sensing from the power supplies to the RPSM module. With a 5 V transient short or problem in the system, the most likely failure mode will be a 5 V output overvoltage fault back at the power supplies. Under high currents the losses will become high enough to cause the voltage at the power supplies to exceed the overvoltage threshold. Refer to the 5 V paragraph in the *Power Supply* section for details. Any time the RPSM P5 green LED is on, the RPSM 5 V output voltage is above 4.55 V.

Redundant power supply replacement - As long as one of the power supplies is fully operational, the RPSM green LEDs will be ON and the correct power will be supplied to the system. When one of the power supplies fails, replacement can be postponed until it is convenient to do so. Before replacing the supply, refer to the troubleshooting guidelines outlined in the *Power Supply* section to rule out a transient fault that can be reset such as an input power undervoltage. If the supply is found to be defective, follow removal and installation procedure outlined in the *Power Supply* section.

Removal and Installation

The RPSM module is mounted to the right hand side of the VME rack on a sheet metal bracket. The status and 28 V dc output connections are at the bottom. Two connectors, PSA and PSB, at the top of the assembly mate with a cable harness carrying power to the VME rack. The four 15-pin Mate-N-Lock connectors at the back side of the module are the primary power feeds from the remotely mounted power supplies.



RPSM Module and VME Chassis



To prevent electric shock, turn off power to the RPSMto be replaced, then test to verify that no power exists on the module before touching it or any connected circuits.



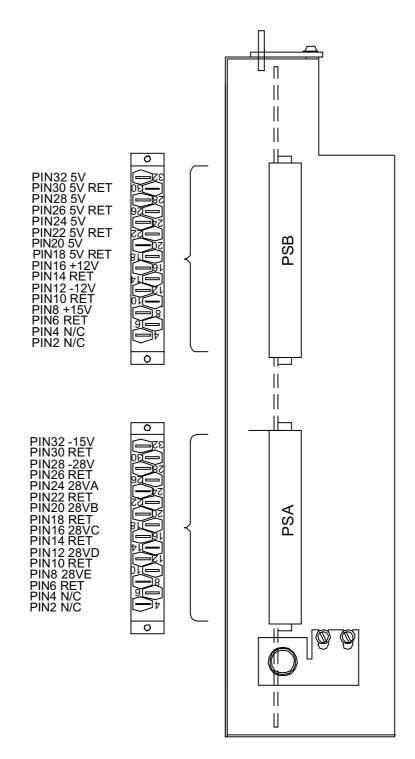
To prevent equipment damage, do not remove, insert, or adjust any connections while power is applied to the equipment.

- > To remove the RPSM (see figures below)
- 1. Loosen the PSA/PSB bracket captive fastener at the top front of the module.
- 2. Separate the PSA/PSB bracket assembly from the RPSM.
- 3. Disconnect the bottom connectors.
- 4. Loosen the two front sheet metal bracket captive fasteners.
- 5. Pull the sheet metal bracket/power module assembly forward, disconnect the four rear side connectors and then slide the assembly off of the control rack.
- 6. Remove the four mounting screws that hold the RPSM to the bracket and remove it.

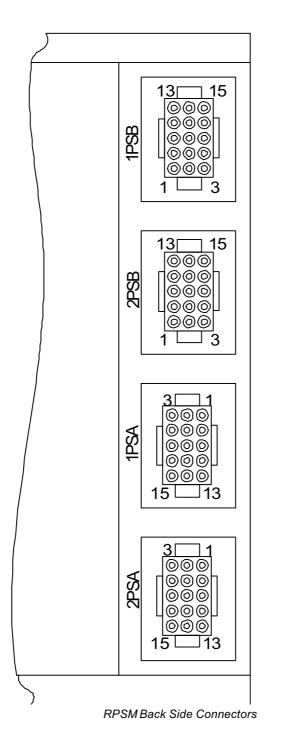
Note Reinstall the screws and bracket on the control rack if a replacement module is not going to be installed.

> To reinstall the RPSM (see figures below)

- 1. Locate the supply mounting sheet metal bracket and four mounting screws.
- 2. Position the module on the bracket with the front of the module at the captive fasteners, then install the four mounting screws and tighten.
- 3. Slide the module bracket assembly on to the control rack, connect the four rear side connectors and then push the assembly in to tighten the two front captive fasteners.
- 4. Slide the PSA/PSB assembly rear tab into the slot on the bracket located at the top rear of the RPSM.
- 5. Push the connector assemble into the mating connectors on the top of the RPSM.
- 6. Tighten the PSA/PSB bracket captive fastener.
- 7. Connect the bottom connectors to the RPSM.

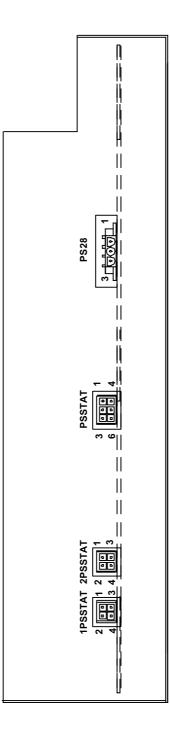


RPSM Top Connectors



	1 & 2PSB
Pin	•
1	P5V1/2
2	P5V1/2
3	P5V1/2
4	P5RTN
5	P5RTN
6	P5RTN
7	NC
8	P5SENP
9	P5SENN
10	P15V1/2
11	N12
12	P12V1/2
13	P15RTN
14	N12RTN1/2
15	P12RTN
- .	1 & 2PSA

Pin • 1 P28AB1/2 2 N28 . 3 N15 . 4 AB28RTN 5 N28RTN1/2 6 N15RTN1/2 7 NC 8 P28AB1/2 9 AB28RTN 10 P28E1/2 P28D1/2 11 12 P28C1/2 E28RTN 13 14 D28RTN 15 C28RTN



Pin	PS28		•
1		P28E	•
2	•	CHASS	•
2	•	E28RTN	•
3	•	EZOKIN	

PSSTAT				
Pin				
1	IDSIG			
4	IDGND			
2	1STAT1			
5	1STAT2			
3	2STAT1			
6	2STAT2			

2PSSTAT

Pin	
1	IDSIG
2	IDGND
3	2STAT1
4	2STAT2

1PSSTAT

Pin	
1	IDSIG
2	IDGND
3	1STAT1
4	1STAT2

GE Industrial Systems

RPSM Bottom Connectors



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GE Industrial Systems

Power Conditioning Boards

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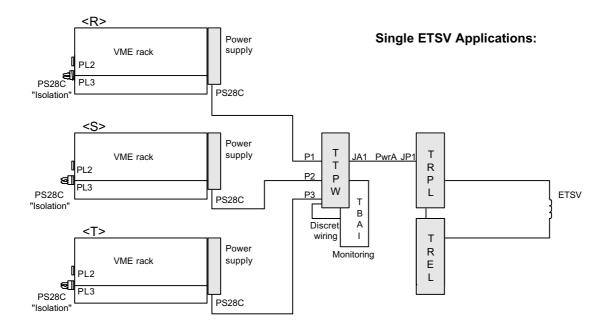
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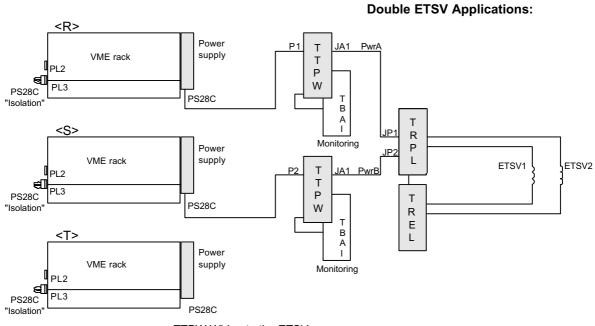
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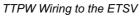
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Functional Description

Large steam turbines use 24 V dc electrical trip solenoid valves (ETSV) board. Power for these valves is provided to the TRPL and TREL trip boards by a power transition board TTPW. Wiring from the rack power supplies, through TTPW, to the trip board is shown in the following figure.

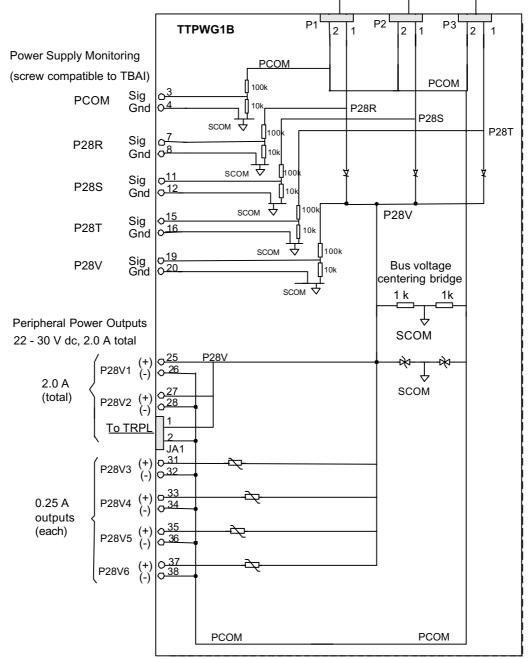






TTPWH1B

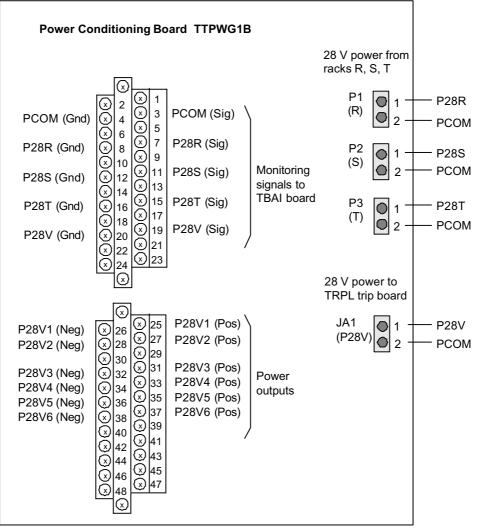
The turbine ETSV is a 24 V dc device with a 24 watt, 20–22 ohm coil. Power is supplied from the three I/O rack supplies to TTPWG1B, where the three 28 V supplies are diode *OR*ed to produce a single 28 V dc output. The primary output is 0 – 2 A (total), 22 - 30 V dc, and there are four secondary outputs of 0.25 A each.



TTPWG1B Board Showing Outputs and Monitoring

Installation

Three 28 V dc supplies are wired from I/O racks R, S, and T to plugs P1, P2, and P3. The primary 28 V dc output comes from plug JA1 and is wired to the trip board TRPL. The power monitoring signals are wired to the top terminal block (TB1) and go to an analog input board. The secondary voltage outputs are wired to the lower terminal block (TB2) as shown in the following figure.



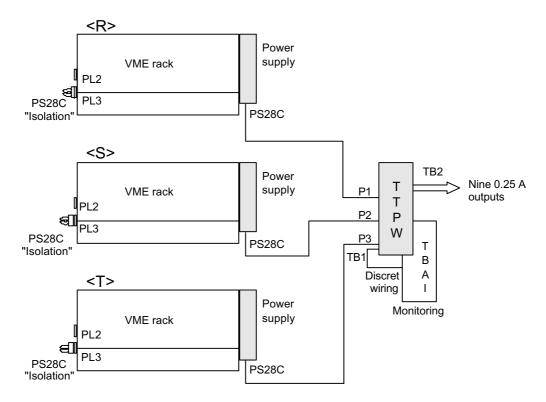
TTPWG1B Board with Wiring and Cabling

TTPWH1A

The TTPWH1A power conditioning board provides branch circuit protection and distribution between one or more Mark VI rack mounted +28 V dc power supplies and discrete wiring to peripheral devices. The H1A has three 2-pin inputs for +28 V dc from the Mark VI power supply. It provides diode *OR* selection between the three inputs to power the +28 V dc outputs. Outputs are rated 22 - 30 V dc, 0 - 0.25 A individually and capable of parallel operation. There is high frequency isolation between the inputs and the outputs and the voltage drop is less than +4 V dc when delivering rated current.

The TTPWH1A internal signal paths are shown in the following figure. Nine current limited 0.25 A outputs are provided and may be paralleled for higher current applications. Typical applications power the H1A from the P28C output of the VME rack power supply. When this is done, the isolation jumper on the rack is placed in the isolated position removing all connections between the P28C output and the rack. The TTPWH1A then provides a resistive bridge to ground to center the power circuit with respect to ground. Voltage feedback monitoring signals are provided using 0.1% resistors allowing monitoring of three input voltages, output voltage, and voltage between PCOM and SCOM.

The +28 V dc power source should have an isolated common (return), especially if the load is external to the cabinet and is grounded. Wiring from the rack power supplies through TTPWH1A to the trip board is shown in the following figure.



TTPWH1A Application Diagram